TEXAS INSTRUMENTS

# TAS5026A

## Six-Channel Digital Audio PWM Processor

PurePath DIGITAL™

# Data Manual

January 2004

DAV Digital Audio/Speaker

SLES068A

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# Contents

## List of Illustrations

## List of Tables

*Table* *Title* *Page*

# 1 Introduction

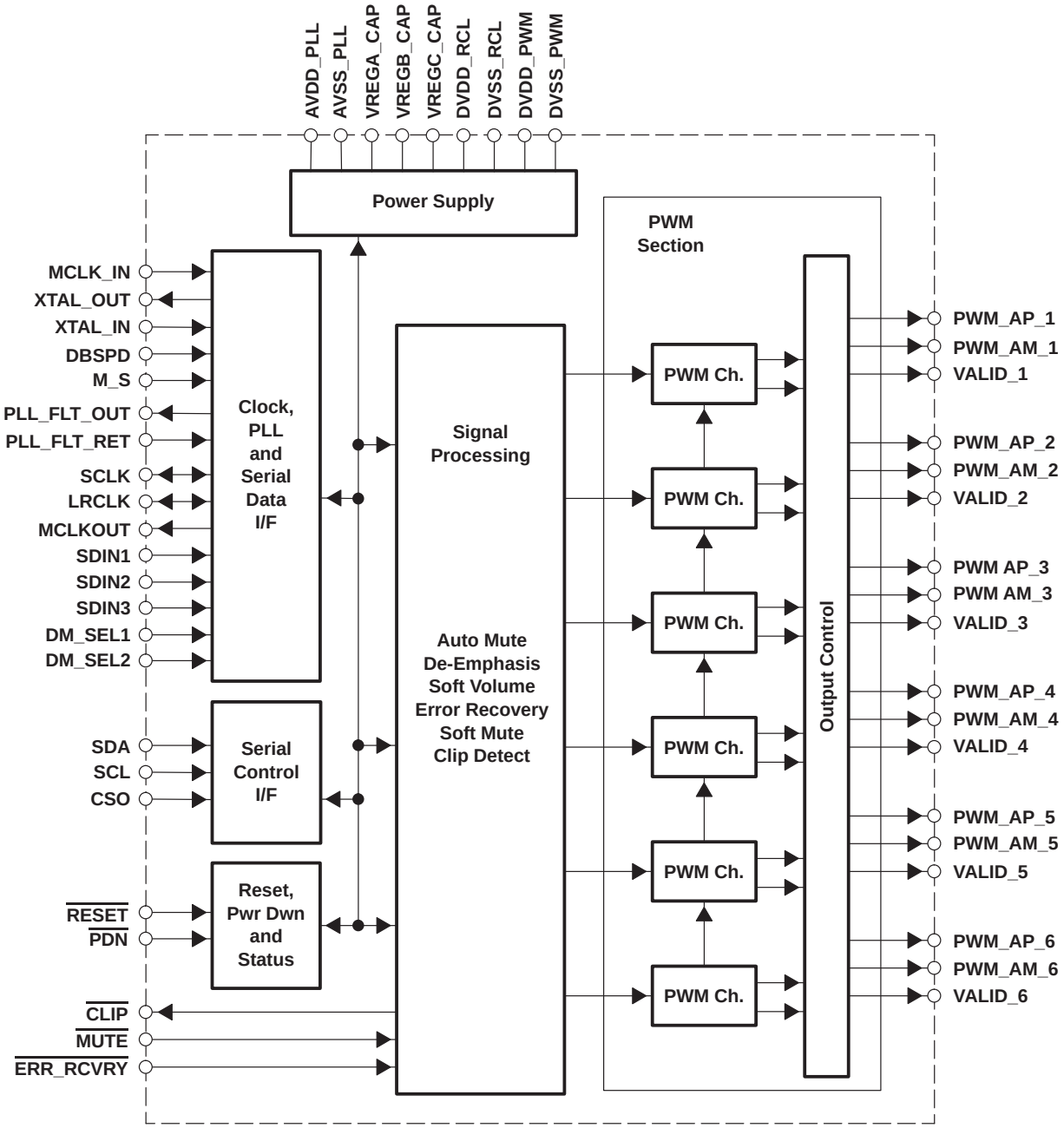
The TAS5026A is an innovative, cost-effective, high-performance 24-bit six-channel digital pulse-width modulator (PWM) based on Equibit™ technology. Combined with a TI PurePath Digital™ audio amplifier power stage, these devices use noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The TAS5026A is designed to drive up to six digital power devices to provide six channels of digital audio amplification. The digital power devices can be six conventional monolithic power stages (such as TAS5110) or six discrete differential power stages using gate drivers and MOSFETs.

The TAS5026A has six independent volume controls and mute. The device operates in AD mode. This all-digital audio system contains only two analog components in the signal chain—an LC low-pass filter at each speaker terminal and can provide up to 96-dB SNR at the speaker terminals. The TAS5026A has a wide variety of serial input options including right justified (16, 20, or 24 bit), I2S (16, 20, or 24 bit) left justified, or DSP (16-bit) data formats. The device is fully compatible with AES standard sampling rates of 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz including de-emphasis for 44.1-kHz and 48-kHz sample rates. The TAS5026A was designed for home theater applications such as DVD minicomponent systems, home theater in a box (HTIB), DVD receiver, A/V receiver, or TV sets.

## 1.1 Features

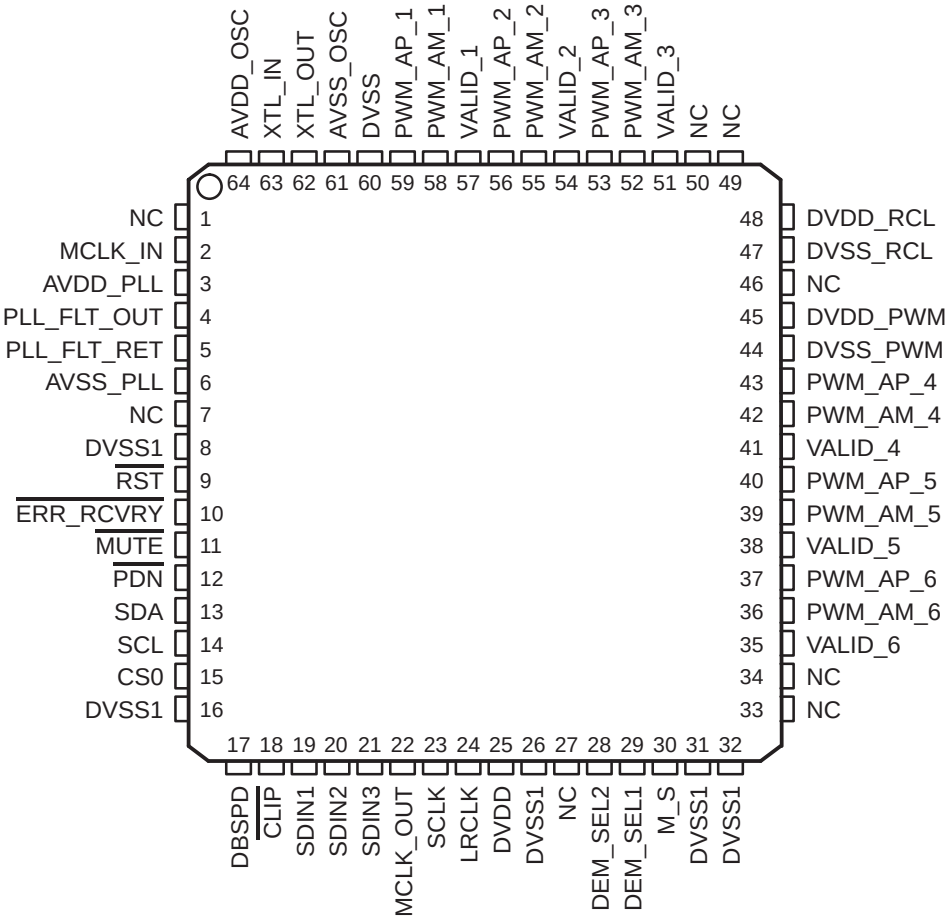
- TI PurePath Digital Audio Amplifier
- High Quality Audio
  - 96-dB SNR
  - <0.1% THD+N
- Six-Channel Volume Control
  - Patented Soft Volume
  - Patented Soft Mute
- 16-, 20-, or 24-Bit Input Data
- Sampling Rates: 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz
- Supports Master and Slave Modes
- 3.3-V Power Supply Operation
- Economical 64-Pin TQFP Package
- Digital De-Emphasis: 32 kHz, 44.1 kHz, and 48 kHz
- Clock Oscillator Circuit for Master Modes
- Low Jitter Internal PLL
- Soft Volume and Mute Update

## 1.2 Functional Block Diagram

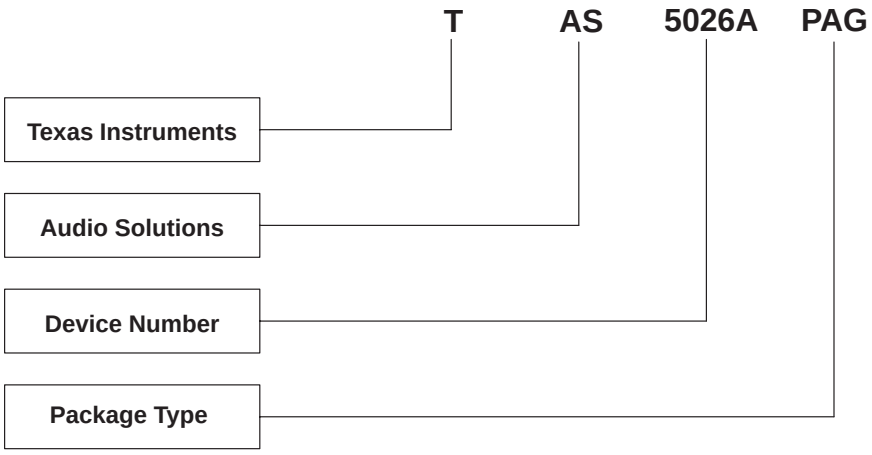


## 1.3 Terminal Assignments

**PAG PACKAGE**
**(TOP VIEW)**



## 1.4 Ordering Information




**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE |
|---|---|
| | PLASTIC 64-PIN TQFP (PAG) |
| 0°C to 70°C | TAS5026APAG |

## 1.5 Terminal Functions

| TERMINAL NAME | TERMINAL NO. | FUNCTION† | DESCRIPTION |
|---|---|---|---|
| AVDD_OSC | 64 | P | Analog power supply for internal oscillator cells |
| AVDD_PLL | 3 | P | 3.3-V analog power supply for PLL |
| AVSS_OSC | 61 | O | Analog ground for internal oscillator cells |
| AVSS_PLL | 6 | P | Analog ground for PLL |
| $\overline{\text{CLIP}}$ | 18 | O | Digital clipping indicator, active low |
| CS0 | 15 | I | $I^2C$ device address select. This is an active high pin. |
| DBSPD | 17 | I | Sample rate is double speed (88.2 kHz or 96 kHz), active high |
| DM_SEL1 | 29 | I | De-emphasis select bit 1 (0 = none, 01 = 32 kHz, 10 = 44.1 kHz |
| DM_SEL2 | 28 | I | De-emphasis select bit 2, 10 = 48 kHz, 11 = undefined (none) |
| DVDD_PWM | 45 | P | 3.3-V digital power supply for PWM |
| DVDD_RCL | 48 | P | 3.3-V digital power supply for re-clocker |
| DVDD | 25 | P | 3.3-V digital power supply for digital core and most of I/O buffers |
| DVSS | 60 | I | Voltage regulator enable, active low |
| DVSS_PWM | 44 | P | Digital ground for PWM |
| DVSS_RCL | 47 | P | Digital ground for re-clocker |
| DVSS1 | 8, 26, 31, 32 | P | Digital ground for digital core and most of I/O buffers |
| $\overline{\text{ERR\_RCVRY}}$ | 10 | I | Error recovery, active low |
| LRCLK | 24 | I/O | Serial audio data left/right clock (sampling rate clock) (input when M_S = 0; output when M_S = 1) |
| M_S | 30 | I | Master/slave mode input signal (master = 1, slave = 0) |
| MCLK_IN | 2 | I | MCLK input, slave mode |
| MCLK_OUT | 22 | O | MCLK output buffered system clock output M_S = 1; otherwise set to 0 |
| $\overline{\text{MUTE}}$ | 11 | I | Mute input signal, active low |

† I = input; O = output; I/O = input/output; P = power

| TERMINAL NAME | TERMINAL NO. | FUNCTION† | DESCRIPTION |
|---|---|---|---|
| NC | 1, 7, 27, 33, 34, 36, 49, 50 | — | No connection |
| $\overline{\text{PDN}}$ | 12 | I | Power down. This signal is active low. |
| PLL_FLT_OUT | 4 | I | PLL external filter |
| PLL_FLT_RET | 5 | I | PLL external filter |
| PWM_AM_1 | 58 | O | PWM 1 output (differential -); {Positive H-bridge side} |
| PWM_AM_2 | 55 | O | PWM 2 output (differential -); {Positive H-bridge side} |
| PWM_AM_3 | 52 | O | PWM 3 output (differential -); {Positive H-bridge side} |
| PWM_AM_4 | 42 | O | PWM 4 output (differential -); {Positive H-bridge side} |
| PWM_AM_5 | 39 | O | PWM 5 output (differential -); {Positive H-bridge side} |
| PWM_AM_6 | 36 | O | PWM 6 output (differential -); {Positive H-bridge side} |
| PWM_AP_1 | 59 | O | PWM 1 output (differential +); {Positive H-bridge side} |
| PWM_AP_2 | 56 | O | PWM 2 output (differential +); {Positive H-bridge side} |
| PWM_AP_3 | 53 | O | PWM 3 output (differential +); {Positive H-bridge side} |
| PWM_AP_4 | 43 | O | PWM 4 output (differential +); {Positive H-bridge side} |
| PWM_AP_5 | 40 | O | PWM 5 output (differential +); {Positive H-bridge side} |
| PWM_AP_6 | 37 | O | PWM 6 output (differential +); {Positive H-bridge side} |
| $\overline{\text{RST}}$ | 9 | I | System reset input. This signal is an active low. |
| SCL | 14 | I | I2C clock signal |
| SCLK | 23 | I/O | Serial audio data clock (master mode = output, slave mode = input) |
| SDA | 13 | I/O | I2C data signal |
| SDIN1 | 19 | I | Serial audio data 1 input |
| SDIN2 | 20 | I | Serial audio data 2 input |
| SDIN3 | 21 | I | Serial audio data 3 input |
| VALID_1 | 57 | O | Output indicating validity of PWM outputs, channel 1, active high |
| VALID_2 | 54 | O | Output indicating validity of PWM outputs, channel 2, active high |
| VALID_3 | 51 | O | Output indicating validity of PWM outputs, channel 3, active high |
| VALID_4 | 41 | O | Output indicating validity of PWM outputs, channel 4, active high |
| VALID_5 | 38 | O | Output indicating validity of PWM outputs, channel 5, active high |
| VALID_6 | 35 | O | Output indicating validity of PWM outputs, channel 6, active high |
| XTL_IN | 63 | I | Crystal or TTL level clock input |
| XTL_OUT | 62 | O | Crystal output (not for external usage) |

† I = input; O = output; I/O = input/output; P = power

# 2 Architecture Overview

The TAS5026A is composed of six functional elements:

- Clock, PLL, and serial data interface ($I^2S$)
- Reset/power-down circuitry
- Serial control interface ($I^2C$)
- Signal processing unit
- Pulse-width modulator (PWM)
- Power supply

## 2.1 Clock and Serial Data Interface

The TAS5026A clock and serial data interface contain an input serial data slave and the clock master/ slave interface. The serial data slave interface receives information from a digital source such as a DSP, S/PDIF receiver, analog-to-digital converter (ADC), digital audio processor (DAP), or other serial bus master. The serial data interface has three serial data inputs that can accept up to six channels of data at data sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. The serial data interfaces support left justified and right justified for 16-, 20-, and 24-bits. In addition, the serial data interface supports the DSP protocol for 16 bits and the $I^2S$ protocol for 24 bits.

The TAS5026A can function as a receiver or a generator for the MCLK_IN (master clock), SCLK (shift clock), and LRCLK (left/right clock) signals that control the flow of data on the three serial data interfaces. The TAS5026A is a clock master when it generates these clocks and is a clock slave when it receives these clocks.

The TAS5026A is a synchronous design that relies upon the master clock to provide a reference clock for all of the device operations and communication via the $I^2C$. When operating as a slave, this reference clock is MCLK_IN. When operating as a master, the reference clock is either a TTL clock input to XTAL_IN or a crystal attached across XTAL_IN and XTAL_OUT.

The clock and serial data interface has two control parameters: data sample rate and clock master or slave.

### *2.1.1 Normal-Speed, Double-Speed, and Quad-Speed Selection*

The data sample rate is selected through a terminal (DBSPD) or the serial control register 0 (X02). The data sample rate control sets the frequencies of the SCLK and LRCLK in clock slave mode and the output frequencies of SCLK and LRCLK in clock master mode. There are three data rates: normal speed, double speed, and quad speed.

Normal-speed mode supports data rates of 32 kHz, 44.1 kHz, and 48 kHz. Normal speed is supported in the master and slave modes. Double-speed mode is used to support sampling rates of 88.2 kHz and 96 kHz. Double speed is supported in master and slave modes. Quad-speed mode is used to support sampling rates of 176.4 kHz and 192 kHz.

The PWM is placed in normal speed by setting the DBSPD terminal low or by setting the normal mode bits in the system control register 0 (x02) through the serial control interface. The PWM is placed in double speed mode by setting the DBSPD terminal high or by setting the double speed bits in the system control register. Quad-speed mode is auto detected supported in slave mode and invoked using the $I^2C$ serial control interface in master mode. In slave mode, if the TAS5026A is not in double speed mode, quad-speed mode is automatically detected when MCLK_IN is 128Fs. In master mode, the PWM is placed in quad-speed mode by setting the quad-speed bit in the system control register through the serial control interface.

If the master clock is well behaved during the frequency transition (the high or low clock periods are not less than 20 ns), then a simple speed selection is simply performed by setting the DBSPD terminal or the serial control register.

When the sample rate is changed, the TAS5026A temporarily suspends processing, places the PWM outputs in a hard mute (PWM P outputs low; PWM M outputs high, and all VALID signals low), resets all internal processes, and suspends all $I^2C$ operations. The TAS5026A then performs a partial re-initialization and noiselessly restarts the PWM output. The TAS5026A preserves all control register settings throughout this sequence. If desired, the sample rate change can be performed while mute is active to provide a completely silent transition. The timing of this control sequence is shown in Section 4.

If the master clock input can encounter a high clock or low clock period of less than 20 ns while the data rates are changing, then $\overline{\text{RESET}}$ should be applied during this time There are two recommended control procedures for this case, depending upon whether the DBSPD terminal or the serial control interface is used. These control sequences are shown in Section 4.

**Table 2−1. Normal-Speed, Double-Speed, and Quad-Speed Operation**

| QUAD-SPEED CONTROL REGISTER BIT | DBSPD TERMINAL OR CONTROL REGISTER BIT | MODE | SPEED SELECTION |
|---|---|---|---|
| 0 | 0 | Master or slave | Normal speed |
| 0 | 1 | Master or slave | Double speed |
| 1 | 0 | Master or slave | Quad speed |
| 0 | 0 | Slave | Quad speed if MCLK_IN = 128 Fs |
| 1 | 1 | Master or slave | Error |

### *2.1.2 Clock Master/Slave Mode (M_S)*

Clock master and slave mode can be invoked using the M_S (master slave) terminal.

This terminal specifies the default mode that is set immediately following a device RESET. The serial data interface setting permits the clock generation mode to be changed during normal operation.

The transition to master mode occurs:

- Following a RESET when M_S terminal has a logic high applied

The transition to slave mode occurs:

- Following a RESET when M_S terminal has a logic low applied

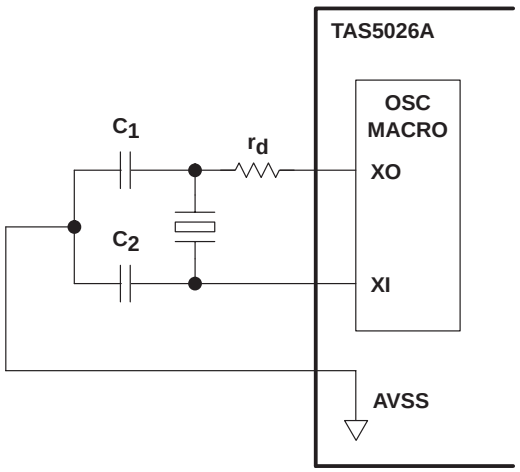
### *2.1.3 Clock Master Mode*

When M_S = 1 following a RESET, the TAS5026A provides the master clock, SCLK, and LRCLK to the rest of the system. In the master mode, the TAS5026A outputs the audio system clocks MCLK_OUT, SCLK, and LRCLK.

The TAS5026A device generates these clocks plus its internal clocks from the internal phase-locked loop (PLL). The reference clock for the PLL can be provided by either an external clock source (attached to XTAL_IN) or a crystal (connected across terminals XTAL_IN and XTAL_OUT). The external source attached to MCLK_IN is 256 times (128 in quad mode) the data sample rate (Fs). The SCLK frequency is 64 times the data sample rate and the SCLK frequency of 48 times the data sample rate is not supported in the master mode. The LRCLK frequency is the data sample rate.

#### 2.1.3.1 Crystal Type and Circuit

In clock master mode the TAS5026A can derive the MCLKOUT, SCLK, and LRCLK from a crystal. In this case, the TAS5026A uses a parallel-mode fundamental-mode crystal. This crystal is connected to the TAS5026A as shown in Figure 2−1.




**$r_d$ = Drive level control resistor − crystal vendor specified**
**$C_L$ = Crystal load capacitance (capacitance of circuitry between the two terminals of the crystal)**
**$C_L = (C_1 \times C_2)/(C_1 + C_2) + C_S$ (where $C_S$ = board stray capacitance ~ 3 pF)**
**Example: Vendor recommended $C_L$ = 18 pF, $C_S$ = 3 pF ≥ $C_1 = C_2 = 2 \times (18-3) = 30$ pF**

**Figure 2−1. Crystal Circuit**

### *2.1.4 Clock Slave Mode*

In the slave mode (M_S = 0), the master clock, LRCLK, and SCLK are inputs to the TAS5026A. The master clock is supplied through the MCLK_IN terminal.

As in the master mode, the TAS5026A device develops its internal timing from the internal phase-locked loop (PLL). The reference clock for the PLL is provided by the input to the MCLK_IN terminal. This input is at a frequency of 256 times (128 in quad mode) the input data rate. The SCLK frequency is 48 or 64 times the data sample rate. The LRCLK frequency is the data sample rate. The TAS5026A does not require any specific phase relationship between SRCLK and MCLK_IN, but there must be synchronization. The TAS5026A monitors the relationship between MCLK, SCLK and LRCLK. The TAS5026A detects if any of the three clocks are absent, if the LRCLK rate changes more than 10 MCLK cycles since the last device reset or clock error, or if the MCLK frequency is changing substantially with respect to the PLL frequency.

When a clock error is detected, the TAS5026A performs a clock error management sequence.

The clock error management sequence temporarily suspends processing, places the PWM outputs in a hard mute (PWM_P outputs are low; PWM_M outputs are high, and all VALID signals are low), resets all internal processes, sets the volumes to mute, and suspends all $I^2C$ operations.

When the error condition is corrected, the TAS5026A exits the clock error sequence by performing a partial re-initialization, noiselessly restarting the PWM output, and ramping the volume up to the level specified in the volume control registers. This sequence is performed over a 60-ms interval. The TAS5026A preserves all control register settings that were set prior to the clock interruption.

If a clock error occurs while the $\overline{\text{ERR\_RCVRY}}$ terminal is asserted (low), the TAS5026A performs the error management sequence up to the unmute sequence. In this case, the volume remains at full attenuation with the PWM output at a 50% duty cycle. The volume can be restored from this latched mute state by triggering a mute/unmute sequence by asserting and releasing $\overline{\text{MUTE}}$ either by using the terminal, the system control register X01 D4, or the individual channel mute register D5−D0.

Alternatively, the TAS5026A can be prevented from entering the latched mute state following a clock error when the $\overline{\text{ERR\_RCVRY}}$ terminal or the error recovery $I^2C$ command (register X03 bit D2) is active by writing x7F to the individual error recovery register (x04) and a x84 to x1F (a feature enable register).

**Table 2−2. Master and Slave Clock Modes**

| DESCRIPTION | M_S | DBSPD | XTL_IN (MHz)† | MCLK_IN (MHz)‡ | SCLK (MHz)☆ | LRCLK (kHz)¶ | MCLK_OUT (MHz)# |
|---|---|---|---|---|---|---|---|
| Internal PLL, master, normal speed | 1 | 0 | 8.192 | - | 2.048 | 32 | 8.192 |
| Internal PLL, master, normal speed | 1 | 0 | 11.2896 | - | 2.8224 | 44.1 | 11.2896 |
| Internal PLL, master, normal speed | 1 | 0 | 12.288 | - | 3.072 | 48 | 12.288 |
| Internal PLL, master, double speed | 1 | 1 | - | 22.5792§ | 5.6448 | 88.2 | 22.5792 |
| Internal PLL, master, double speed | 1 | 1 | - | 24.576§ | 6.144 | 96 | 24.576 |
| Internal PLL, master, quad speed | 1 | 0 | - | 22.5792 | 11.2896 | 176.4 | 22.5792 |
| Internal PLL, master, quad speed | 1 | 0 | - | 24.576 | 12.288 | 192 | 24.576 |
| Internal PLL, slave, normal speed | 0 | 0 | - | 8.192§ | 2.0484 | 32 | Digital GND |
| Internal PLL, slave, normal speed | 0 | 0 | - | 11.2896§ | 2.8224 | 44.1 | Digital GND |
| Internal PLL, slave, normal speed | 0 | 0 | - | 12.288§ | 3.072 | 48 | Digital GND |
| Internal PLL, slave, double speed | 0 | 1 | - | 22.5792 | 5.6448 | 88.2 | Digital GND |
| Internal PLL, slave, double speed | 0 | 1 | - | 24.576§ | 6.144 | 96 | Digital GND |
| Internal PLL, slave, quad speed ‖ | 0 | 0 | - | 22.5792§ | 11.2896 | 176 | Digital GND |
| Internal PLL, slave, quad speed ‖ | 0 | 0 | - | 24.576§ | 12.288 | 192 | Digital GND |

† A crystal oscillator is connected to XTL_IN.
‡ MCLK_IN tied low when input to XTL_IN is provided; XTL_IN tied low when MCLK_IN_IN is provided.
§ External MCLK_IN connected to MCLK_IN_IN input
¶ SCLK and LRCLK are outputs when M_S = 1, and inputs when M_S = 0.
# MCLK_OUT is driven low when M_S = 0.
‖ Quad-speed mode is detected automatically.
☆SCLK can be 48 or 64 times Fs

**Table 2−3. LRCLK and MCLK_IN Rates**

| | NORMAL SPEED (kHz) | | | | DOUBLE SPEED (kHz) | | | | QUAD SPEED (kHz) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LRCLK | **1 Fs** | **32** | **44.1** | **48** | **1 Fs** | **64** | **88.2** | **96** | **1 Fs** | **176.4** | **192** |
| MCLK_IN | **256 Fs** | 8,192 | 11,289.6 | 12,288 | **256 Fs** | 16,384 | 22,579.2 | 24,576 | **128 Fs** | 22,579.2 | 24,576 |

### 2.1.5 PLL External Filter

A low jitter PLL produces the internal timing of the TAS5026A (when in master mode), the master clock, SCLK, and LRCLK. Connections for the PLL external filter are provided through PLL_FLT_OUT and PLL_FLT_RET as shown in Figure 2−2.

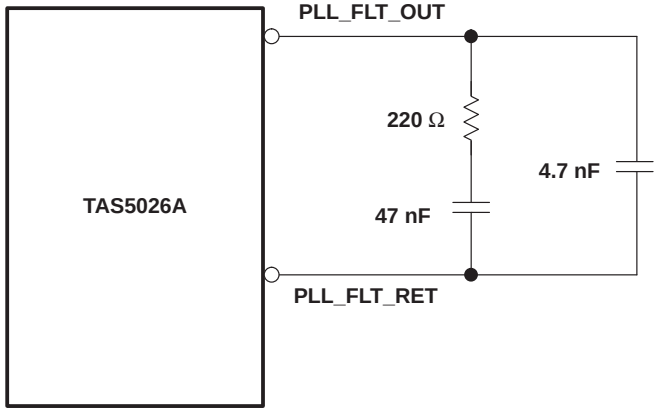



**Figure 2−2. PLL External Filter**

### 2.1.6 DCLK

DCLK is the internal high frequency clock that is produced by the PLL circuitry from MCLK. The TAS5026A uses the DCLK to control all internal operations. DCLK is 8 times the speed of MCLK in normal speed mode, 4 times MCLK in double speed, and 2 times MCLK in quad speed. With respect to the $I^2C$ addressable registers, DCLK clock cycles are used to specify interchannel delay and to detect when the MCLK frequency is drifting. Table 2−4 DCLK shows the relationship between Sample Rate, MCLK, and DCLK.

**Table 2−4. DCLK**

| Fs (kHz) | MCLK (MHz) | DCLK (MHz) | DCLK Period (ns) |
|---|---|---|---|
| 32 | 8.1920 | 65.5360 | 15.3 |
| 44.1 | 11.2896 | 90.3168 | 11.1 |
| 48 | 12.2880 | 98.3040 | 10.2 |
| 88 | 22.5280 | 90.1120 | 11.1 |
| 96 | 24.5760 | 98.3040 | 10.2 |
| 192 | 49.1520 | 98.3040 | 10.2 |

### 2.1.7 Serial Data Interface

The TAS5026A operates as a slave only/receive only serial data interface in all modes. The TAS5026A has three PCM serial data interfaces to accept six channels of digital data though the SDIN1, SDIN2, SDIN3 inputs. The serial audio data is in MSB first; 2s complement format.

The serial data interfaces of the TAS5026A can be configured in right justified, $I^2S$, left-justified, or DSP modes. This interface supports 32-kHz, 44.1-kHz, 48-kHz, 88-kHz, 96-kHz, 176.4-kHz, and 192-kHz data sample rates. The serial data interface format is specified using the data interface control register. The supported word lengths are shown in Table 2−5.

During normal operating conditions if the serial data interface settings change state, an error recovery sequence is initiated.

**Table 2−5. Supported Word Lengths**

| DATA MODES | WORD LENGTHS | MOD2 | MOD1 | MOD0 |
|---|---|---|---|---|
| Right justified, MSB first | 16 | 0 | 0 | 0 |
| Right justified, MSB first | 20 | 0 | 0 | 1 |
| Right justified, MSB first | 24 | 0 | 1 | 0 |
| $I^2S$ | 16 | 0 | 1 | 1 |
| $I^2S$ | 20 | 1 | 0 | 0 |
| $I^2S$ | 24 | 1 | 0 | 1 |
| Left justified, MSB first | 24 | 1 | 1 | 0 |
| DSP frame | 16 | 1 | 1 | 1 |

### 2.1.7.1 I²S Timing

I²S timing uses an LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The LRCLK is low for the left channel and high for the right channel. A bit clock running at 48 or 64 times Fs is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS5026A masks unused trailing data bit positions. Master mode only supports a 64 times Fs bit clock.

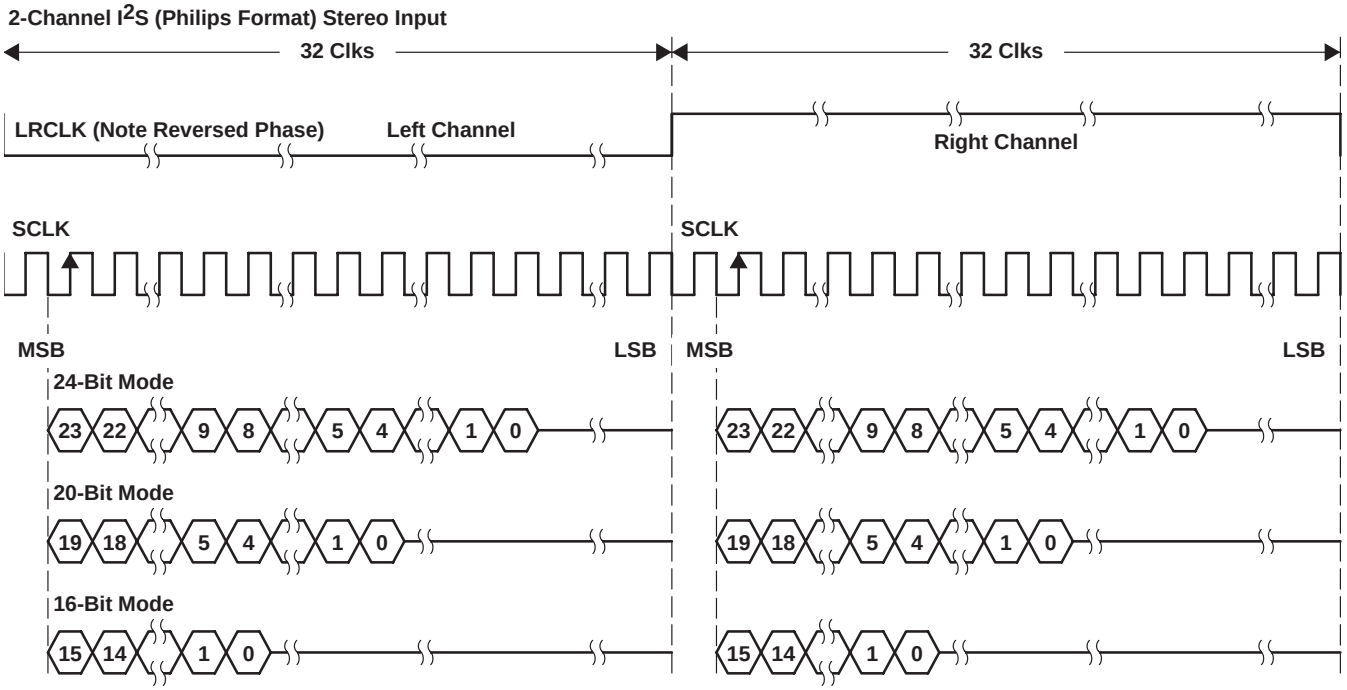



**Figure 2−3. I²S 64-Fs Format**

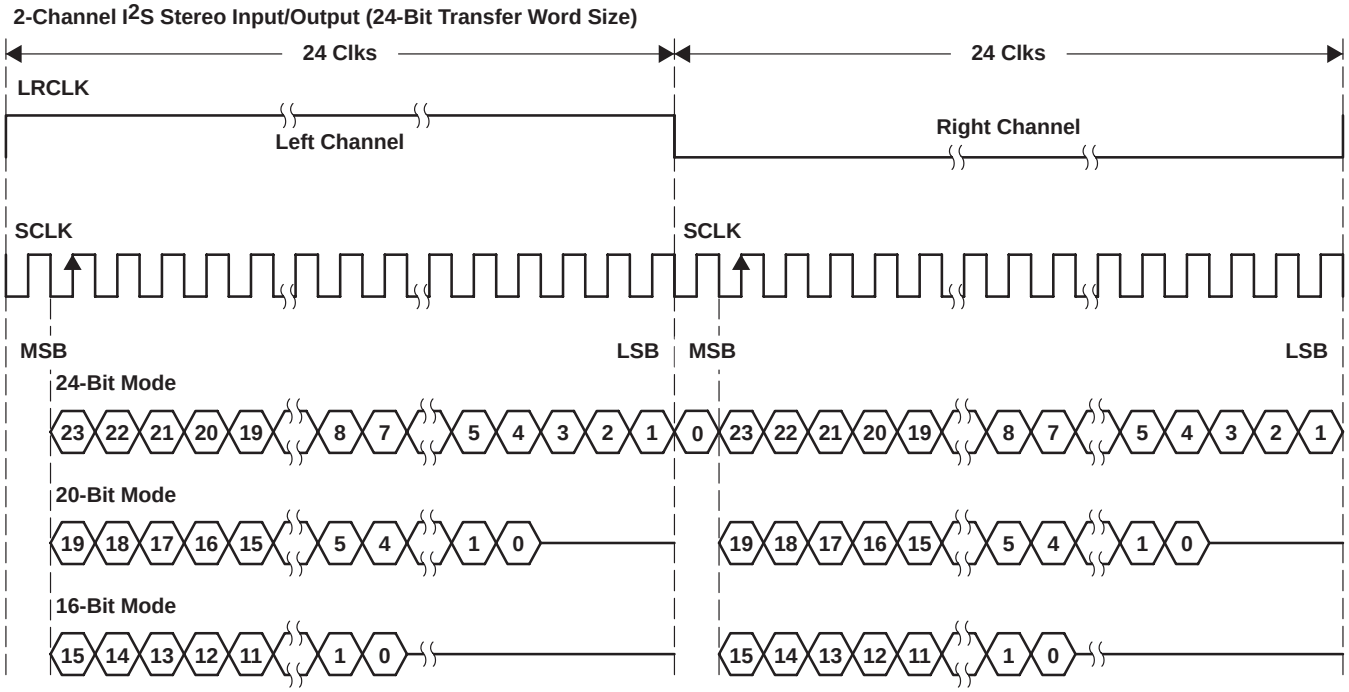
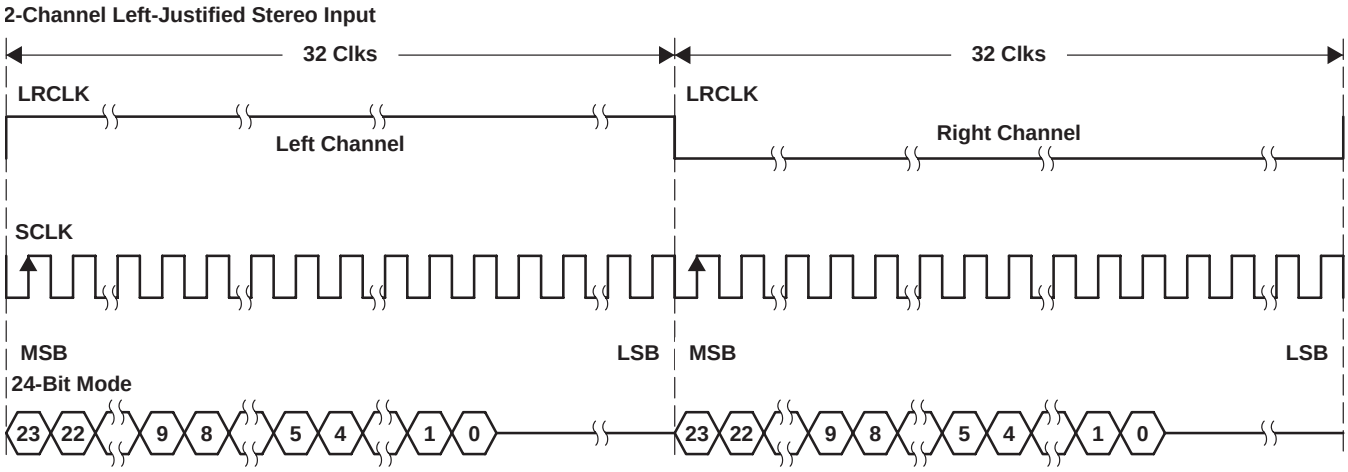



**Figure 2−4. I²S 48-Fs Format**

### 2.1.7.2 Left-Justified Timing

Left-justified (LJ) timing uses an LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The LRCLK is high for the left channel and low for the right channel. A bit clock running at 48 or 64 times Fs is used to clock in the data. The first bit of data appears on the data lines at the same time the LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS5026A masks unused trailing data bit positions. Master mode only supports a 64 times Fs bit clock.




NOTE: All data presented in 2s complement form with MSB first.

**Figure 2−5. Left-Justified 64-Fs Format**

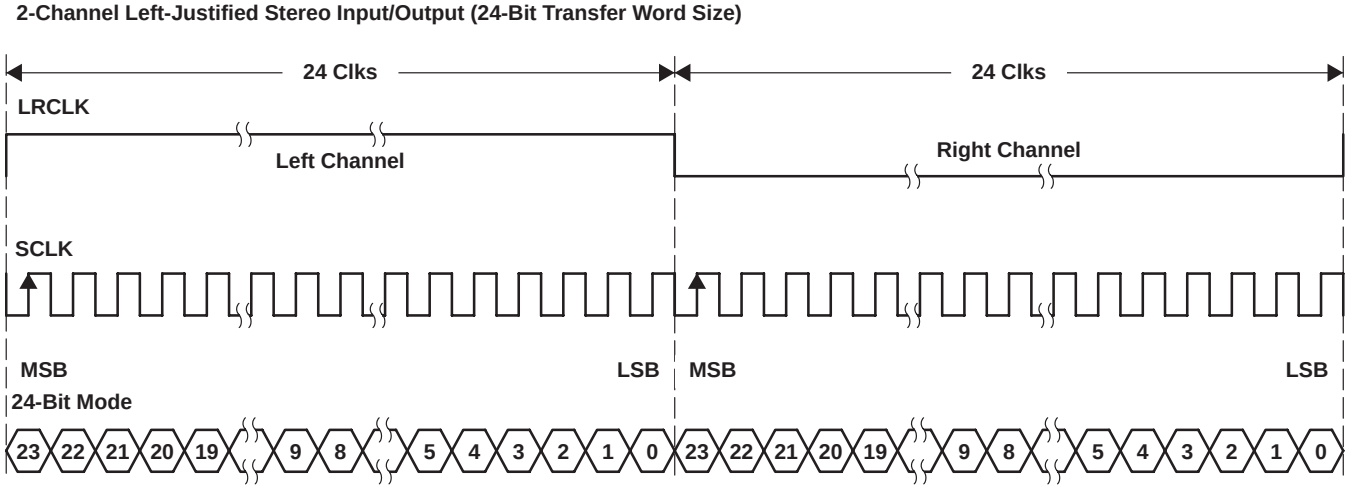
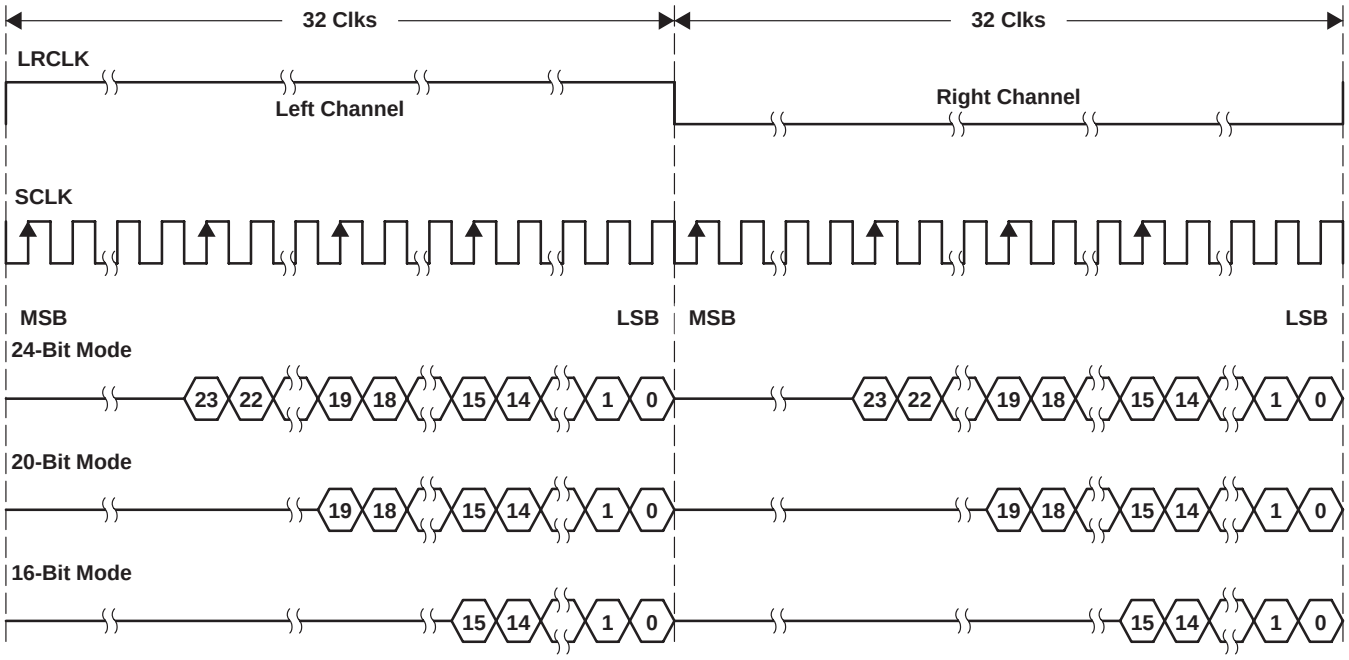



**Figure 2−6. Left-Justified 48-Fs Format**

### 2.1.7.3 Right-Justified Timing

Right-justified (RJ) timing uses an LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The LRCLK is high for the left channel and low for the right channel. A bit clock running at 48 or 64 times Fs is used to clock in the data. The first bit of data appears on the data 8-bit clock periods (for 24-bit data) after LRCLK toggles. In RJ mode, the last bit clock before LRCLK transitions always clocks the LSB of data. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS5026A masks unused leading data bit positions. Master mode only supports a 64 times Fs bit clock.

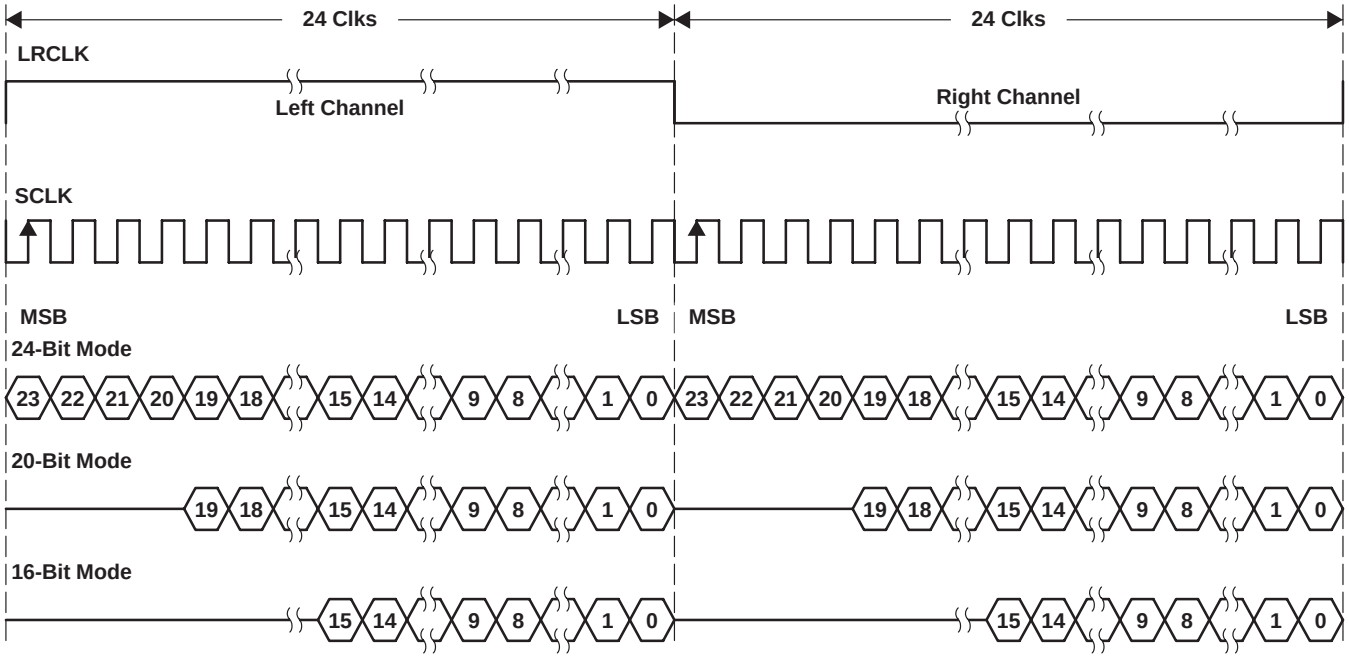
**2-Channel Right-Justified (Sony Format) Stereo Input**




NOTE: All data presented in 2s complement form with MSB first.

**Figure 2−7. Right-Justified 64-Fs Format**

**2-Channel Right-Justified Stereo Input/Output (24-Bit Transfer Word Size)**




NOTE: All data presented in 2s complement form with MSB first.

**Figure 2−8. Right-Justified 48-Fs Format**

#### 2.1.7.4 DSP Mode Timing

DSP mode timing uses an LRCLK to define when data is to be transmitted for both channels. A bit clock running at 64 × Fs is used to clock in the data. The first bit of the left channel data appears on the data lines following the LRCLK transition. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS5026A masks unused trailing data bit positions.

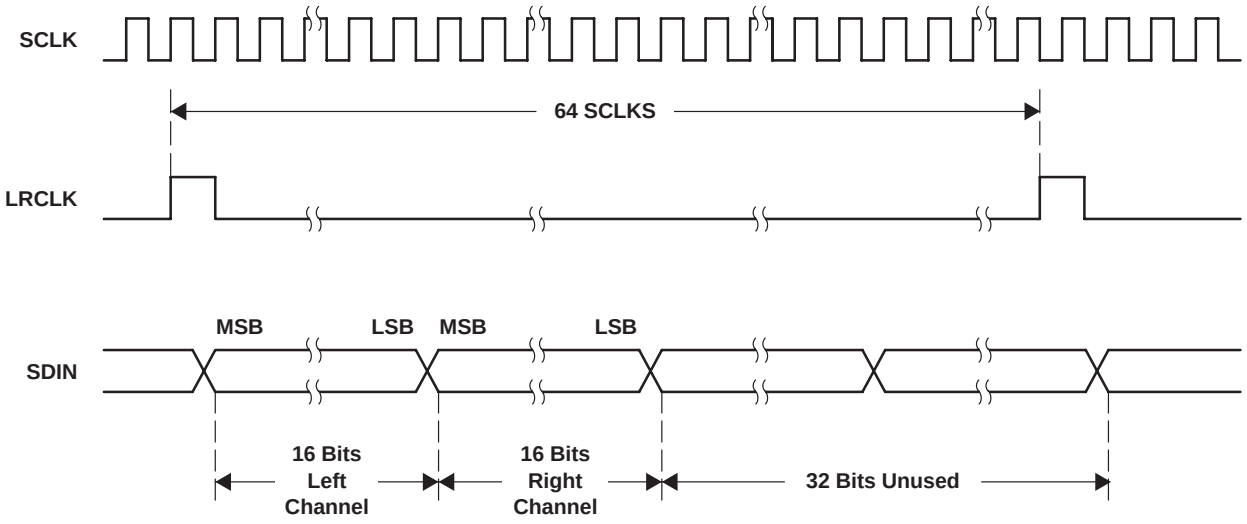



**Figure 2−9. DSP Format**

## 2.2 Reset, Power Down, and Status

The reset, power down, and status circuitry provides the necessary controls to bring the TAS5026A to the initial inactive condition, achieve low power standby, and report system status.

### *2.2.1 Reset—$\overline{RESET}$*

The TAS5026A is placed in the reset mode by setting the $\overline{\text{RESET}}$ terminal low.

$\overline{\text{RESET}}$ is an asynchronous control signal that restores the TAS5026A to its default conditions, sets the valid 1−6 outputs low, and places the PWM in the hard mute state. Volume is immediately set to full attenuation (there is no ramp down).

As long as the $\overline{\text{RESET}}$ terminal is held low, the device is in the reset state. During reset, all $I^2C$ and serial data bus operations are ignored. Table 2−6 shows the device output signals while $\overline{\text{RESET}}$ is active.

Upon the release of $\overline{\text{RESET}}$, if POWER_DWN is high, the system performs a 4-ms to 5-ms device initialization and then ramps the volume up to 0 db using a soft volume update sequence. If MCLK_IN is not active when RESET is released high, then a 4-ms to 5-ms initialization sequence is produced once MCLK_IN becomes active.

During device initialization all controls are reset to their initial states. Table 2−7 shows the control settings that are changed during initialization.

$\overline{\text{RESET}}$ should be applied during power-up initialization or while changing the master slave clock states.

**Table 2−6. Device Outputs During Reset**

| SIGNAL | MODE | SIGNAL STATE |
|---|---|---|
| Valid 1−Valid 6 | All | Low |
| PWM P-outputs | All | Low |
| PWM M-outputs | All | Low |
| MCLKOUT | All | Low |
| SCLK | Master | Low |
| SCLK | Slave | Signal input |
| LRCLK | Master | Low |
| LRCLK | Slave | Signal input |
| SDA | All | Signal input |
| $\overline{\text{CLIP}}$ | All | High |

Because the $\overline{\text{RESET}}$ is an asynchronous control signal, small clicks and pops can be produced during the application (the leading edge) of this control. However, when $\overline{\text{RESET}}$ is released, the transition from the hard mute state back to normal operation is performed synchronously using a quiet sequence.

If a completely quiet reset sequence is desired, $\overline{\text{MUTE}}$ should be applied before applying $\overline{\text{RESET}}$.

**Table 2−7. Values Set During Reset**

| CONTROL | SETTING |
|---|---|
| Volume | 0 dB |
| MCLK_IN frequency | 256 |
| Master/slave mode | M_S terminal state |
| Automute | Enabled |
| De-emphasis | None |
| DC offset | 0 |
| Interchannel delay | Each channel is set to a default value |

### *2.2.2 Power Down—$\overline{\text{PDN}}$*

The TAS5026A can be placed into the power-down mode by holding the $\overline{\text{PDN}}$ terminal low. When power-down mode is entered, both the PLL and the oscillator are shut down. Volume is immediately set to full attenuation (there is no ramp down). The valid 1−6 outputs are immediately asserted low and the PWM outputs are placed in the hard mute state. $\overline{\text{PDN}}$ initiates device power down without clock inputs. As long as the $\overline{\text{PDN}}$ terminal is held low—the device is in the power-down (hard mute) state.

During power down, all $I^2C$ and serial data bus operations are ignored. Table 2−8 shows the device output signals while $\overline{\text{PDN}}$ is active.

**Table 2−8. Device Outputs During Power Down**

| SIGNAL | MODE | SIGNAL STATE |
|---|---|---|
| Valid 1−Valid 6 | All | Low |
| PWM P-outputs | All | Low |
| PWM M-outputs | All | Low |
| MCLKOUT | All | Low |
| SCLK | Master | Low |
| SCLK | Slave | Signal input |
| LRCLK | Master | Low |
| LRCLK | Slave | Signal input |
| SDA | All | Signal input |
| $\overline{\text{CLIP}}$ | All | High |

To place the device in total power-down mode, both RESET and power-down modes must be enabled. Prior to bringing $\overline{\text{PDN}}$ high, $\overline{\text{RESET}}$ must be brought low for a minimum of 50 ns.

Because $\overline{\text{PDN}}$ is an asynchronous control signal, small clicks and pops can be produced during the application (the leading edge) of this control. However, when $\overline{\text{PDN}}$ is released, the transition from the hard mute state back to normal operation is performed synchronously using a quiet sequence.

If a completely quiet reset sequence is desired, $\overline{\text{MUTE}}$ should be applied before applying $\overline{\text{PDN}}$.

#### 2.2.2.1 Recovery Time Options

To support the requirements of various system configurations, the TAS5026A can come up to the normal state after either a long (100 ms) or a short (5 ms) delay.

1. In the first case, a slow system (95 ms to 100 ms) start-up occurs at the end of the power-down sequence when:

   $\overline{\text{RESET}}$ is high for at least 16 MCLK_IN periods before $\overline{\text{PDN}}$ goes high.

2. Otherwise a fast (4 ms to 5 ms) start-up occurs.

   **NOTE:** If MCLK_IN is not active when both of these signals are released high, then a fast (4 ms to 5 ms) start-up occurs once MCLK_IN becomes active.

### *2.2.3 General Status Registers*

The general status register is a read only register. This register provides an indication when a volume update is in progress or one of the channels is inactive. The device id can be read using this register.

**Volume update is in progress—**Whenever a volume change is in progress due to a volume update command or mute, this status bit is high.

**Device identification code—**The device identification code, 1 0011, is displayed.

**No internal errors (all valid signals are high)—**When there are no internal errors in the TAS5026A and all outputs are valid, this status bit is high.

**One or more valid signals are inactive—**If low, one or more channels of the TAS5026A are not outputting data. The Valid signals for those channels are inactive.

This can be produced by one of three causes:

- One or more of the clock signals are in error
- $\overline{\text{Error}}$ recover is active (low)
- The automute has silenced one or more channels that are receiving 0 inputs
- $\overline{\text{Mute}}$ has been set
- Volume control has been set to full attenuation

If this signal is high, the TAS5026A is outputting data on all channels.

### *2.2.4 Error Status Register*

The error status register indicates historical information on control signal changes and clock errors. This register latches these indications when they occur. The indications are cleared by writing a 00(Hex) to the register.

This register is intended as a diagnostic tool to be used only when the system is not operating correctly. This is because the error status bits are set when the data rate, serial data interface format, or master/slave mode is changed. As a result, this register indicates an error condition even though the system is operating normally. This register should only be used while diagnosing transient error conditions.

Any clock error or control signal terminal change which occurs since the last time the error status register was cleared is displayed. In using this register, the first step is to initialize the device and verify that all of the clock signals are active. Then this register should be cleared by writing a 00(Hex). At this point, the register indicates any errors or control signal changes.

This register indicates an error condition by a high for the following conditions:

- FS ERROR
- A control terminal change has occurred ($\overline{M\_S}$, DBLSPD)
- LRCLK error
- MCLK_IN count error
- DCLK phase error with respect to MCLK_IN
- MCLK_IN phase error with respect to DCLK
- PWM timing error

If all bits of the register are low, no errors have occurred and no control terminals changed.

There is no one-to-one correspondence of clock error indication to a system error condition. A particular system error can be indicated by one or more error indications in this register. The system error conditions and the reported errors are as follows:

There is no correct number of MCLKs per LRCLK:

- FS error has occurred
- LRCLK error
- MCLK_IN count error

LRCLK is absent:

- LRCLK error

MCLK is the wrong frequency, changing frequency, or absent:

- DCLK phase error with respect to MCLK
- MCLK phase error with respect to DCLK
- PWM timing error

SCLK is the wrong frequency or absent:

- SCLK error

## 2.3 Signal Processing

This section contains the signal processing functions that are contained in the TAS5026A. The signal processing is performed using a high-speed 24-bit signal processing architecture. The TAS5026A performs the following signal processing features:

- Individual channel soft volume with a range of 24 dB to −114 dB plus mute
- Soft mute
- Automute
- 50-µs/15-µs de-emphasis filter supported in the sampling rates 32 kHz, 44.1 kHz, and 48 kHz

### *2.3.1 Volume Control*

The gain of each output can be adjusted by a soft digital volume control for each channel. Volume adjustments are performed using a soft gain update s-curve, which is approximated using a second order filter fit. The curve fit is performed over a transition interval between 41 ms and 65 ms.

The volume of each channel can be adjusted from mute to −114 dB to 24 dB in 0.5 dB steps. Because of the numerical representation that is used to control the volume, at very low volume levels the step size increases for gains that are less than −96 dB. The default volume setting following power up or reset is 0 dB for all channels. The step size adjustment is linear down to approximately −90 dB, see see Figure 2−10.

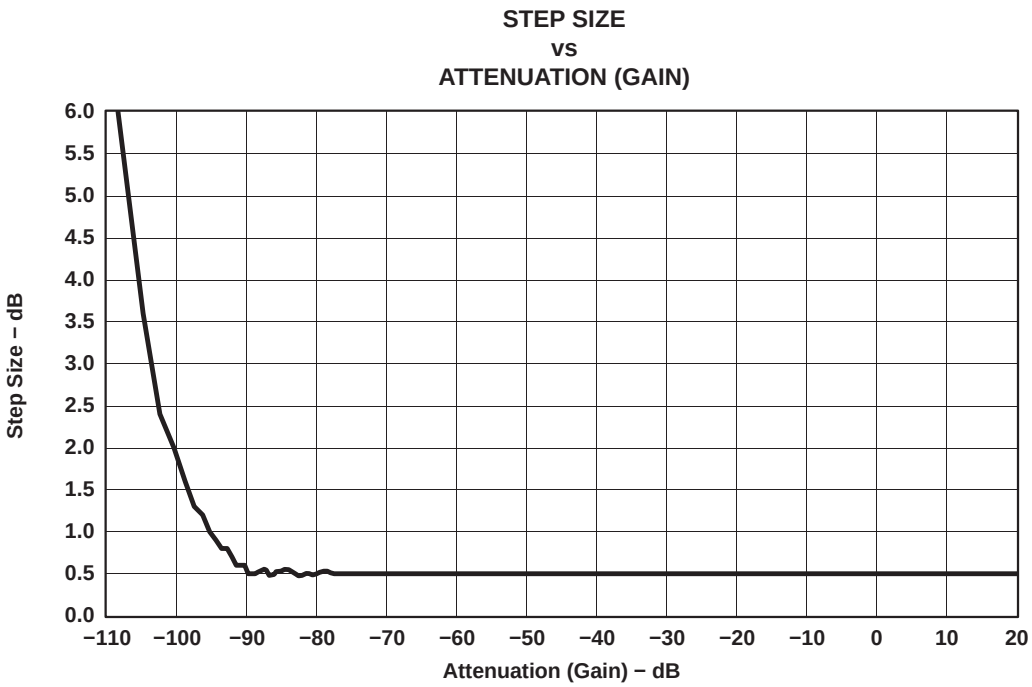



**Figure 2−10. Attenuation Curve**

The volume control format for each channel is expressed in 8 bits. The volume for each channel is set by writing 8 bits via the serial control interface. The MSB bit is written first as in the bit position 0 (LSB position).

The volume for each channel can be set using a single or multiple address write operation to the volume control register via the serial control interface. Changing the volume of all six channels requires that 6 registers be updated.

To coordinate the volume adjustment of multiple channels simultaneously, the TAS5026A performs a delayed volume update upon receiving a volume change command. Following the completion of the register volume write operations, the TAS5026A waits for 5 ms for another volume command to be given. If no volume command is issued in that period of time, the TAS5026A starts adjusting the volume of the channels that received volume settings.

While a volume update is being performed, the system status register indicates that the update is in progress. During the update, all subsequent volume control setting requests that are sent to the TAS5026A are received and stored as a single next value for a subsequent update. If more than one volume setting request is sent, only the last is retained.

**Table 2−9. Volume Register**

| VOLUME REGISTER | | | | | | | |
|---|---|---|---|---|---|---|---|
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Vol Bit 7 | Vol Bit 6 | Vol Bit 5 | Vol Bit 4 | Vol Bit 3 | Vol Bit 2 | Vol Bit 1 | Vol Bit 0 |

### *2.3.2 Mute*

The application of mute ramps the volume from any setting to noiseless hard mute state. There are two methods in which the TAS5026A can be placed into mute. The TAS5026A is placed in the noiseless mute when the $\overline{\text{MUTE}}$ terminal is asserted low for a minimum of 3 MCLK_IN cycles. Alternatively, the mute mode can be initiated by setting the mute bit in the system control register through the serial control interface. The TAS5026A is held in mute state as long as the terminal is low or $I^2C$ mute setting is active. This command uses quiet entry and exit sequences to and from the hard mute state.

If an error recovery (described in the PWM section) occurs after a mute request has been received, the device returns from error recovery with the channel volume set as specified by the mute command.

### 2.3.3 Automute

Automute is an automatic sequence that can be enabled or disabled via the serial control interface. The default for this control is enabled. When enabled, the PWM automutes an individual channel when a channel receives from 5 ms to 50 ms of consecutive zeros. This time interval can be selectable using the automute delay register. The default interval is 5 ms at 48 kHz. This duration is independent of the sample rate. The automute state is exited when two consecutive samples of nonzero data are received. The TAS5026A exit from automute is performed quickly and preserves all music information.

This mode uses the valid low to provide a low-noise floor while maintaining a short start-up time. Noise free entry and exit is achieved by using the PWM quiet start and stop sequences.

### 2.3.4 Individual Channel Mute

Individual channel mute is invoked through the serial interface. Individual channel mute permits each channel of the TAS5026A to be individually muted and unmuted. The operation that is performed is identical to the mute operation; however, it is performed on a per channel basis. A TAS5026A channel is held in the mute state as long as the serial interface mute setting for that channel is set.

### 2.3.5 De-Emphasis Filter

For audio sources that have been pre-emphasized, a precision 50-µs/15-µs de-emphasis filter is provided to support the sampling rates of 32 kHz, 44.1 kHz, and 48 kHz. See Figure 2−11 for a graph showing the de-emphasis filtering characteristics. De-emphasis is set using two bits in the system control register.

**Table 2−10. De-Emphasis Filter Characteristics**

| DEM_SEL2 (MSB) | DEM_SEL1 | DESCRIPTION |
|---|---|---|
| 0 | 0 | De-emphasis disabled |
| 0 | 1 | De-emphasis enabled for Fs = 48 kHz |
| 1 | 0 | De-emphasis enabled for Fs = 44 kHz |
| 1 | 1 | De-emphasis enabled for Fs = 32 kHz |

Following the change of state of the de-emphasis bits, the PWM outputs go into the soft mute state. After 128 LRCLK periods for initialization, the PWM outputs are driven to the normal (unmuted) mode.

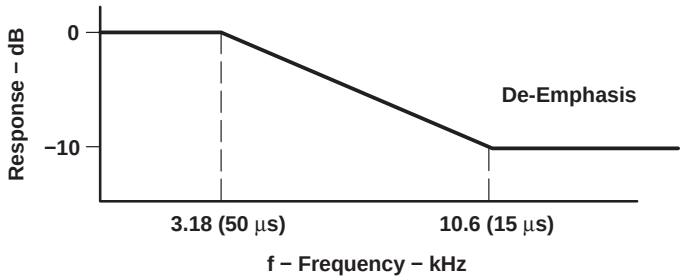



**Figure 2−11. De-Emphasis Filter Characteristics**

## 2.4 Pulse-Width Modulator (PWM)

The TAS5026A contains six channels of high performance digital Equibit PWM modulators that are designed to drive switching output stages (back ends) in both single-ended (SE) and H-bridge (bridge tied load) configuration. The TAS5026A device uses noise shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction.

The PWM provides six pseudo-differential outputs to drive six monolithic power stages (such as TAS5110) or six discrete differential power stages using of gate drivers (such as the TAS5182) and MOSFETs in single-ended or bridged configurations. The TAS5026A also provides a high performance differential output that can be used to drive an external analog headphone amplifier.

### 2.4.1 Clipping Indicator

The clipping output is designed to indicate clipping. When any of the six PWM outputs exceeds the maximum allowable amplitude, the clipping indicator is asserted. The clipping indicator is cleared every 10 ms.

### 2.4.2 Error Recovery

Error recovery is used to provide error management and to permit the PWM output to be reset while preserving all intervolume, interchannel delay, dc offsets, and the other internal settings. Error recovery is initiated by bringing the $\overline{\text{ERR\_RCVRY}}$ terminal low for a minimum 5 MCLK_IN cycles or by setting the error recovery bit in control register 1. Error recovery is a level sensitive signal.

The device also performs an error recovery automatically:

- When the speed configuration is changed to normal, double, or quad speed
- Following a change in the serial data bus interface configuration

When $\overline{\text{ERR\_RCVRY}}$ is brought low, all valid signals go low, and the PWM-P and PWM-M outputs go low. If there are any pending speed configurations, these changes are then performed. When $\overline{\text{ERR\_RCVRY}}$ is brought high, a delay of 4 ms to 5 ms is performed before the system starts the output re-initialization sequence. After the initialization time, the TAS5026A begins normal operation. During error recovery, all controls and device settings that were not updated are maintained in their current configurations.

To permit error recovery to be used to provide TAS5100 error management and recovery, the delay between the start of (falling edge) error recovery and the falling edge of valid 1 though valid 6 is selectable. This delay can be selected to be either 6 μs or 47 μs.

During error recovery all serial data bus operations are ignored. At the conclusion of the sequence, the error recovery register bit is returned to normal operation state. Table 2−11 shows the device output signal states while during error recovery.

**Table 2−11. Device Outputs During Error Recovery**

| SIGNAL | MODE | SIGNAL STATE |
|---|---|---|
| Valid 1−Valid 6 | All | Low |
| PWM P-outputs | All | Low |
| PWM M-outputs | All | Low |
| MCLKOUT | All | Low |
| SCLK | Master | Low |
| SCLK | Slave | Signal input |
| LRCLK | Master | Low |
| LRCLK | Slave | Signal input |
| SDA | All | Signal input |
| $\overline{\text{CLIP}}$ | All | High |

The transitions are done using a quiet entrance and exit sequence to prevent pops and clicks.

### 2.4.3 Individual Channel Error Recovery

Individual channel error recovery is used to provide error management and to permit the PWM output to be turned off. Error recovery is initiated by setting one or more of the six error recovery bits in the error recovery register to low.

While the error recover bits are brought low, the valid signals go to the low state. When the error recovery bits are brought high, a delay of 4 ms to 5 ms occurs before the channels are returned to normal operation.

The delay between the falling edge of the error recover bit and the falling edge of valid 1 though valid 6 is selectable. This delay can be selected to be either 6 μs or 47 μs.

The TAS5026A controls the relative timing of the pseudo-differential drive control signals plus the valid signal to minimize the production of system noise during error recovery operations. The transitions to valid low and valid high are done using an almost quiet entrance and exit sequence to prevent pops and clicks.

### 2.4.4 PWM DC-Offset Correction

An 8-bit value can be programmed to each of the six PWM offset correction registers to correct for any offset present in the output stages. The offset correction is divided into 256 intervals with a total offset correction of ±1.56% of full scale. The default value is zero correction represented by 00 (hex). These values can be changed at any time through the serial control interface.

### 2.4.5 Interchannel Delay

An 8-bit value can be programmed to each of the six PWM interchannel delay registers to add a delay per channel from 0 to 255 clock cycles. The delays correspond to cycles of the high-speed internal clock, DCLK. Each subsequent channel has a default value that is N DCLKs larger than the preceding channel. The default values are 0 for the first channel and 76 for each successive channel.

These values can be updated upon power up through the serial control interface. This delay is generated in the PWM block with the appropriate control signals generated in the CTL block.

These values can be changed at any time through the serial control interface.

**NOTE:**

The performance of a PurePath Digital™ amplifier system is optimized by setting the PWM timing based upon the type of back-end device that is used and the layout. These values are set during initialization using the $I^2C$ serial interface.

### 2.4.6 PWM/H-Bridge and Discrete H-Bridge Driver Interface

The TAS5026A provides six PWM outputs, which are designed to drive switching output stages (back-ends) in both single-ended (SE) and H-bridge (bridge tied load) configuration. The back-ends may be monolithic power stages (such as the TAS5110) or six discrete differential power stages using gate drivers (such as the the TAS55182) and MOSFETs in single-ended or bridged configurations.

The TAS5110 device is optimized for bridge tied load (BTL) configurations. These devices require a pure differential PWM signal with a third signal (VALID) to control the MUTE state. In the MUTE state, the TAS5110 OUTA and OUTB are both low.

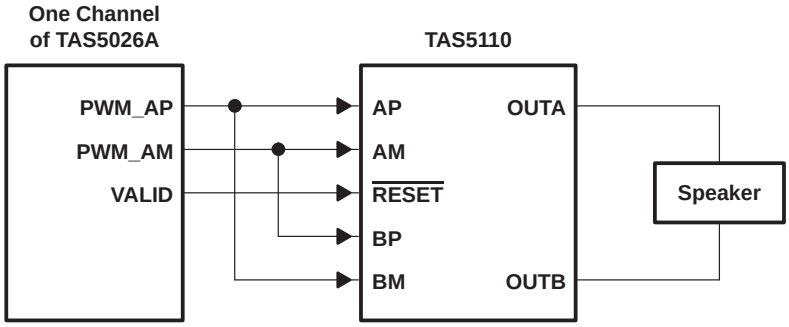



**Figure 2−12. PWM Outputs and H-Bridge Driven in BTL Configuration**

## 2.5 $I^2C$ Serial Control Interface

MCLK must be active for the TAS5026A to support $I^2C$ bus transactions. The TAS5026A has a bidirectional serial control interface that is compatible with the $I^2C$ (Inter IC) bus protocol and supports both 100 KBPS and 400 kbps data transfer rates for single and multiple byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The TAS5026A supports the standard-mode $I^2C$ bus operation (100 kHz maximum) and the fast $I^2C$ bus operation (400 kHz maximum). The TAS5026A performs all $I^2C$ operations without $I^2C$ wait cycles.

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The I2C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data are transferred in byte (8 bit) format with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 2−13. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TAS5026A holds SDA low during acknowledge clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. I2C An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

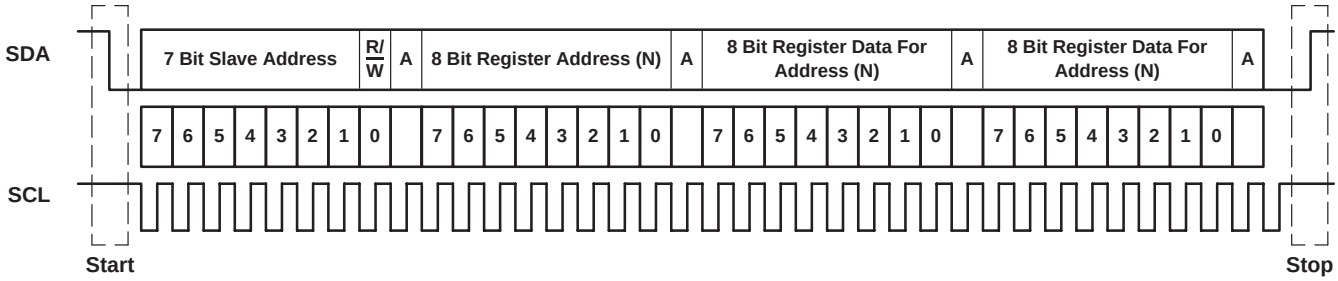



**Figure 2−13. Typical I2C Sequence**

There are no limits on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is also shown in Figure 2−13.

The 7-bit address for the TAS5026A is 001101X, where X is a programmable address bit. Using the CS0 terminal on the device, the LSB address bit is programmable to permit two devices to be used in a system. These two addresses are licensed I2C addresses and do not conflict with other licensed I2C audio devices. To communicate with the TAS5026A, the I2C master uses 0011010 if CS0 = 0 and 0011011 if CS0 = 1. In addition to the 7-bit device address, an 8-bit register address is used to direct communication to the proper register location within the device interface.

Read and write operations to the TAS5026A can be done using single byte or multiple byte data transfers.

### *2.5.1 Single-Byte Write*

As shown in Figure 2−14, a single byte data write transfer begins with the master device transmitting a start condition followed by the I2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is 0. After receiving the correct I2C device address and the read/write bit, the TAS5026A device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5026A internal memory address being accessed. After receiving the address byte, the TAS5026A again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5026A again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single byte data write transfer.

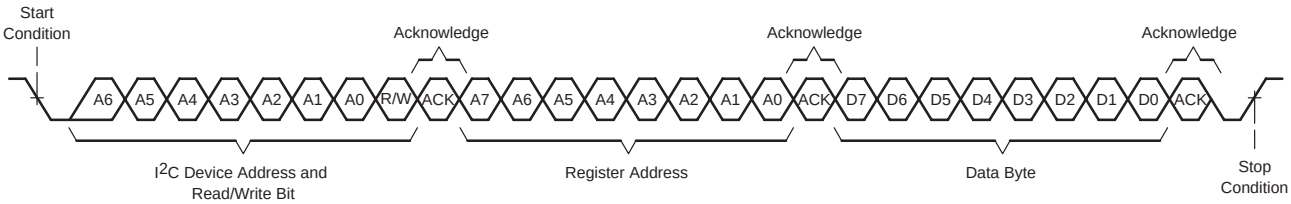



**Figure 2−14. Single-Byte Write Transfer**

## 2.5.2 Multiple-Byte Write

A multiple byte data write transfer is identical to a single byte data write transfer except that multiple data bytes are transmitted by the master device to TAS5026A as shown in Figure 2−15. After receiving each data byte, the TAS5026A responds with an acknowledge bit.

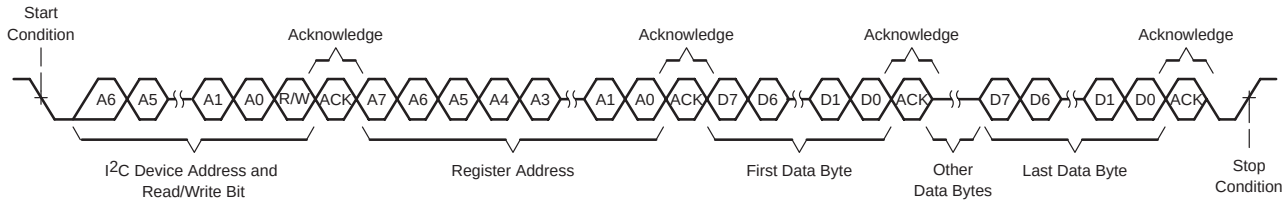



**Figure 2−15. Multiple-Byte Write Transfer**

## 2.5.3 Single-Byte Read

As shown in Figure 2−16, a single byte data read transfer begins with the master device transmitting a start condition followed by the I2C device address and the read/write bit. For the data read transfer, a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is 0. After receiving the TAS5026A address and the read/write bit, the TAS5026A responds with an acknowledge bit. Also, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5026A address and the read/write bit again. This time the read/write bit is a 1 indicating a read transfer. After receiving the TAS5026A and the read/write bit, the TAS5026A again responds with an acknowledge bit. Next, the TAS5026A transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

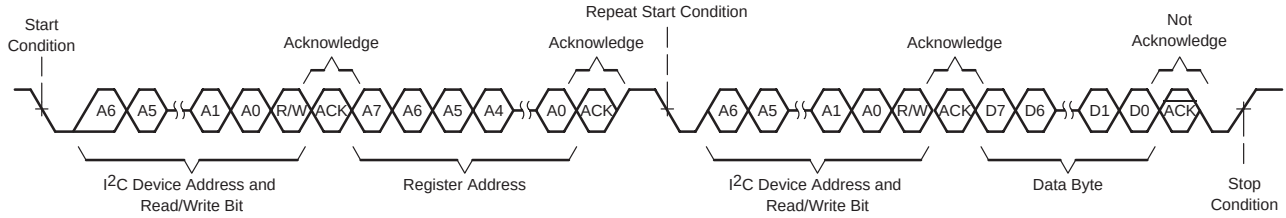



**Figure 2−16. Single-Byte Read**

## 2.5.4 Multiple-Byte Read

A multiple byte data read transfer is identical to a single byte data read transfer except that multiple data bytes are transmitted by the TAS5026A to the master device as shown in Figure 2−17. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

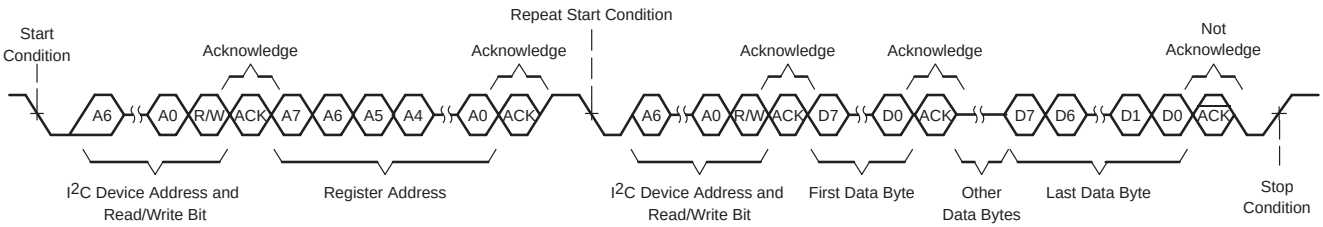



**Figure 2−17. Multiple-Byte Read**

# 3 Serial Control Interface Register Definitions

Table 3−1 shows the register map for the TAS5026A. Default values in this section are in bold.

**Table 3−1. $I^2C$ Register Map**

| ADDR HEX | DESCRIPTION |
|---|---|
| 00 | General status register |
| 01 | Error status register |
| 02 | System control register 0 |
| 03 | System control register 1 |
| 04 | Error recovery register |
| 05 | Automute delay |
| 06 | DC-offset control register channel 1 |
| 07 | DC-offset control register channel 2 |
| 08 | DC-offset control register channel 3 |
| 09 | DC-offset control register channel 4 |
| 0A | DC-offset control register channel 5 |
| 0B | DC-offset control register channel 6 |
| 0C | Interchannel delay register channel 1 |
| 0D | Interchannel delay register channel 2 |
| 0E | Interchannel delay register channel 3 |
| 0F | Interchannel delay register channel 4 |
| 10 | Interchannel delay register channel 5 |
| 11 | Interchannel delay register channel 6 |
| 12 | Reserved |
| 13 | Volume control register channel 1 |
| 14 | Volume control register channel 2 |
| 15 | Volume control register channel 3 |
| 16 | Volume control register channel 4 |
| 17 | Volume control register channel 5 |
| 18 | Volume control register channel 6 |
| 19 | Individual channel mute |

The volume table is contained in Appendix A.

Default values are shown in bold in the following tables.

## 3.1 General Status Register (0x00)

**Table 3−2. General Status Register (Read Only)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | No volume update is in progress. |
| 1 | - | - | - | - | - | - | - | Volume update is in progress. |
| **-** | **0** | **-** | **-** | **-** | **-** | **-** | **-** | Always 0 |
| **-** | **-** | **1** | **0** | **0** | **1** | **1** | **-** | Device identification code |
| - | - | - | - | - | - | - | 0 | Any valid signal is inactive (see status register (0x03)) (see Note 1). |
| **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | No internal errors (all valid signals are high) |

NOTE 1: This bit is reset automatically when one or more channels are active.

## 3.2 Error Status Register (0x01)

**Table 3−3. Error Status Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 1 | - | - | - | - | - | - | - | FS error has occurred |
| - | 1 | - | - | - | - | - | - | Control pin change has occurred |
| - | - | - | 1 | - | - | - | - | LRCLK error |
| - | - | - | - | 1 | - | - | - | MCLK_IN count error |
| - | - | - | - | - | 1 | - | - | DCLK phase error with respect to MCLK_IN |
| - | - | - | - | - | - | 1 | - | MCLK_IN phase error with respect to DCLK |
| - | - | - | - | - | - | - | 1 | PWM timing error |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | No errors—no control pins changed |

NOTE 2: Write 00 hex to clear error indications in error status register.

## 3.3 System Control Register 0 (0x02)

**Table 3−4. System Control Register 0**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **-** | **-** | **-** | **-** | **-** | **-** | Normal mode (in slave mode—quad speed detected if MCLK_IN = 128 Fs) |
| 0 | 1 | - | - | - | - | - | - | Double speed |
| 1 | 0 | - | - | - | - | - | - | Quad speed |
| 1 | 1 | - | - | - | - | - | - | Illegal |
| **-** | **-** | **0** | **-** | **-** | **-** | **-** | **-** | Use de-emphasis pin controls |
| - | - | 1 | - | - | - | - | - | Use de-emphasis I2C controls |
| **-** | **-** | **-** | **0** | **0** | **-** | **-** | **-** | No de-emphasis |
| - | - | - | 0 | 1 | - | - | - | De-emphasis for Fs = 32 kHz |
| - | - | - | 1 | 0 | - | - | - | De-emphasis for Fs = 44.1 kHz |
| - | - | - | 1 | 1 | - | - | - | De-emphasis for Fs = 48 kHz |
| - | - | - | - | - | 0 | 0 | 0 | 16 bit, MSB first; right justified |
| - | - | - | - | - | 0 | 0 | 1 | 20 bit, MSB first; right justified |
| - | - | - | - | - | 0 | 1 | 0 | 24 bit, MSB first; right justified |
| - | - | - | - | - | 0 | 1 | 1 | 16-bit $I^2S$ |
| - | - | - | - | - | 1 | 0 | 0 | 20-bit $I^2S$ |
| **-** | **-** | **-** | **-** | **-** | **1** | **0** | **1** | 24-bit $I^2S$ |
| - | - | - | - | - | 1 | 1 | 0 | 16-bit MSB first |
| - | - | - | - | - | 1 | 1 | 1 | 16-bit DSP Frame |

## 3.4 System Control Register 1 (0x03)

**Table 3−5. System Control Register 1**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | Reserved |
| - | 0 | - | - | - | - | - | - | Valid remains high during automute. |
| **-** | **1** | **-** | **-** | **-** | **-** | **-** | **-** | Valid goes low during automute. |
| - | - | 0 | - | - | - | - | - | Valid remains high during mute. |
| **-** | **-** | **1** | **-** | **-** | **-** | **-** | **-** | Valid goes low during mute. |
| - | - | - | 0 | - | - | - | - | Mute |
| **-** | **-** | **-** | **1** | **-** | **-** | **-** | **-** | Normal mode |
| - | - | - | - | 0 | - | - | - | Set error recovery delay at 6 μs |
| **-** | **-** | **-** | **-** | **1** | **-** | **-** | **-** | Set error recovery delay at 47 μs |
| - | - | - | - | - | 0 | - | - | Error recovery (forces error recovery initialization sequence) |
| **-** | **-** | **-** | **-** | **-** | **1** | **-** | **-** | Normal mode |
| - | - | - | - | - | - | 0 | - | Automute disabled |
| **-** | **-** | **-** | **-** | **-** | **-** | **1** | **-** | Automute enabled |
| **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | Reserved |

## 3.5 Error Recovery Register (0x04)

**Table 3−6. Error Recovery Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | **1** | **–** | **–** | **–** | **–** | **–** | **–** | Set to 11 under default conditions and when x00 is written into 0x1F |
| 0 | – | – | – | – | – | – | – | if 0x84 is written into 0x1F –<br>Enable volume ramp up after an error recovery sequence initiated by the $\overline{\text{ERR\_RCVRY}}$ terminal or the $I^2C$ error recovery command (register 0x03 bit D2). |
| 1 | – | – | – | – | – | – | – | if 0x84 is written into 0x1F –<br>Disable volume ramp up after an error recovery sequence initiated by the $\overline{\text{ERR\_RCVRY}}$ terminal or the $I^2C$ error recovery command (register 0x03 bit D2) |
| – | 0 | – | – | – | – | – | – | if 0x84 is written into 0x1F –<br>Enable volume ramp up after error recovery sequence initiated by register bits D5–D0 of this register. |
| – | 1 | – | – | – | – | – | – | if 0x84 is written into 0x1F –<br>Enable volume ramp up after error recovery sequence initiated by register bits D5–D0 of this register. |
| – | – | 0 | – | – | – | – | – | Put channel 6 into error recovery mode |
| – | – | – | 0 | – | – | – | – | Put channel 5 into error recovery mode |
| – | – | – | – | 0 | – | – | – | Put channel 4 into error recovery mode |
| – | – | – | – | – | 0 | – | – | Put channel 3 into error recovery mode |
| – | – | – | – | – | – | 0 | – | Put channel 2 into error recovery mode |
| – | – | – | – | – | – | – | 0 | Put channel 1 into error recovery mode |
| **–** | **–** | **1** | **1** | **1** | **1** | **1** | **1** | Normal operation |

## 3.6 Automute Delay Register (0x05)

**Table 3−7. Automute Delay Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **-** | **-** | **-** | **-** | Reserved |
| **-** | **-** | **-** | **-** | **0** | **0** | **0** | **0** | Set automute delay at 5 ms |
| - | - | - | - | 0 | 0 | 0 | 1 | Set automute delay at 10 ms |
| - | - | - | - | 0 | 0 | 1 | 0 | Set automute delay at 15 ms |
| - | - | - | - | 0 | 0 | 1 | 1 | Set automute delay at 20 ms |
| - | - | - | - | 0 | 1 | 0 | 0 | Set automute delay at 25 ms |
| - | - | - | - | 0 | 1 | 0 | 1 | Set automute delay at 30 ms |
| - | - | - | - | 0 | 1 | 1 | 0 | Set automute delay at 35 ms |
| - | - | - | - | 0 | 1 | 1 | 1 | Set automute delay at 40 ms |
| - | - | - | - | 1 | - | - | 0 | Set automute delay at 45 ms |
| - | - | - | - | 1 | - | - | 1 | Set automute delay at 50 ms |

## 3.7 DC-Offset Control Registers (0x06−0x0B)

Channels 1, 2, 3, 4, 5, and 6 are mapped into (0x06, 0x07, 0x08, 0x09, 0x0A, and 0x0B).

**Table 3−8. DC-Offset Control Registers**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Maximum correction for positive dc offset (–1.56% FS) |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | No dc-offset correction |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Maximum correction for negative dc offset (1.56% FS) |

## 3.8 Interchannel Delay Registers (0x0C−0x11)

Channels 1, 2, 3, 4, 5, and 6 are mapped into (0x0C, 0x0D, 0x0E, 0x0F, 0x10, and 0x11).

The first channel delay is set at 0. Each subsequent channel has a default value that is 76 DCLKs larger than the preceding channel.

**Table 3−9. Six Interchannel Delay Registers**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | Minimum absolute delay, 0 DCLK cycles, default for channel 1 |
| **0** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | Default for channel 2 |
| **1** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | Default for channel 3 |
| **1** | **1** | **1** | **0** | **0** | **1** | **0** | **0** | Default for channel 4 |
| **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | Default for channel 5 |
| **0** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | Default for channel 6 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Maximum absolute delay, 255 DCLK cycles |

## 3.9 Individual Channel Mute Register (0x19)

**Table 3−10. Individual Channel Mute Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | **1** | - | - | - | - | - | - | Reserved |
| **-** | **-** | **1** | **1** | **1** | **1** | **1** | **1** | No channels are muted |
| - | - | - | - | - | - | - | 0 | Mute channel 1 |
| - | - | - | - | - | - | 0 | - | Mute channel 2 |
| - | - | - | - | - | 0 | - | - | Mute channel 3 |
| - | - | - | - | 0 | - | - | - | Mute channel 4 |
| - | - | - | 0 | - | - | - | - | Mute channel 5 |
| - | - | 0 | - | - | - | - | - | Mute channel 6 |

# 4 System Procedures for Initialization, Changing Data Rates, and Switching Between Master and Slave Modes

## 4.1 System Initialization

Reset is used during system initialization to hold the TAS5026A inactive while power (VDD), the master clock (MCLK_IN), the device control, and the data signals become stable. The recommended initialization sequence is to hold $\overline{\text{RESET}}$ low for 24 MCLK_IN cycles after VDD has reached 3 V and the other control signals ($\overline{\text{MUTE}}$, $\overline{\text{PDN}}$, M_S, $\overline{\text{ERR\_RCVRY}}$, DBSPD, and CS0) are stable.

Figure 4−1 shows the recommended sequence and timing for the $\overline{\text{RESET}}$ terminal relative to system VDD voltage and MCLK.

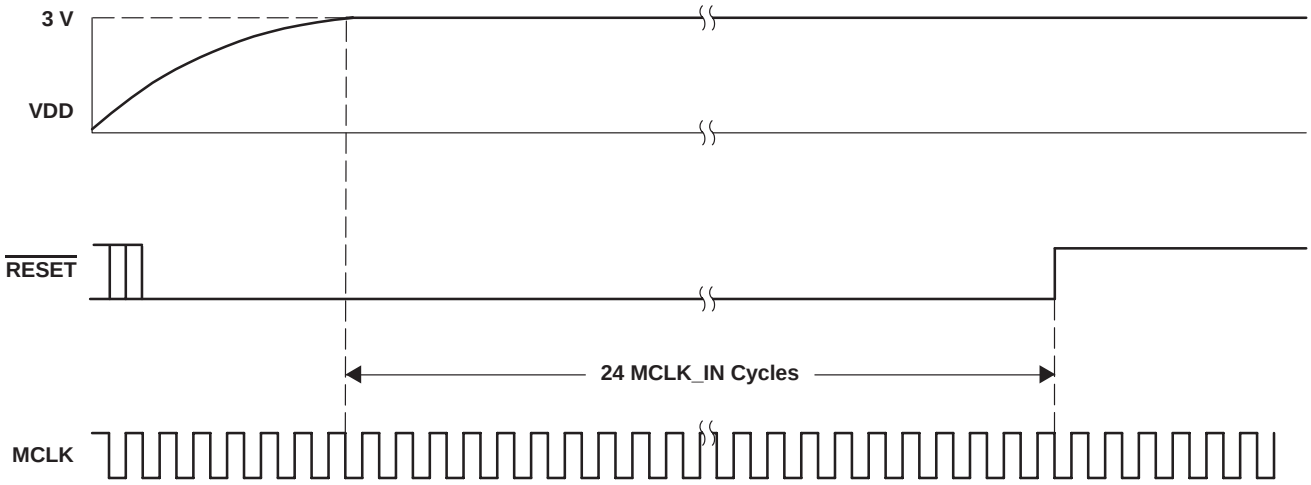



**Figure 4−1. $\overline{\text{RESET}}$ During System Initialization**

Within the first 2 ms following the low to high transition of the $\overline{\text{RESET}}$ terminal, the serial data interface format should be set in the serial data interface control register using the $I^2C$ serial control interface. If the data rate setting is other than the setting specified by the DBSPD terminal, then the data rate should be set using the DBSPD terminal or $I^2C$ interface within 2 ms, following the low to high transition of the $\overline{\text{RESET}}$ terminal.

The time available to set the $I^2C$ registers following the low to high transition of the $\overline{\text{RESET}}$ terminal can be extended using the $\overline{\text{ERR\_RCVRY}}$ terminal. While $\overline{\text{ERR\_RCVRY}}$ is low, the TAS5026A outputs are held inactive. Once the $I^2C$ control registers are set, the $\overline{\text{ERR\_RCVRY}}$ terminal can be released and the TAS5026A starts operation. Figure 4−2 shows how $\overline{\text{ERR\_RCVRY}}$ terminal can be used to extend the interval as long as necessary to set the $I^2C$ registers following the low-to-high transition of the $\overline{\text{RESET}}$ terminal.

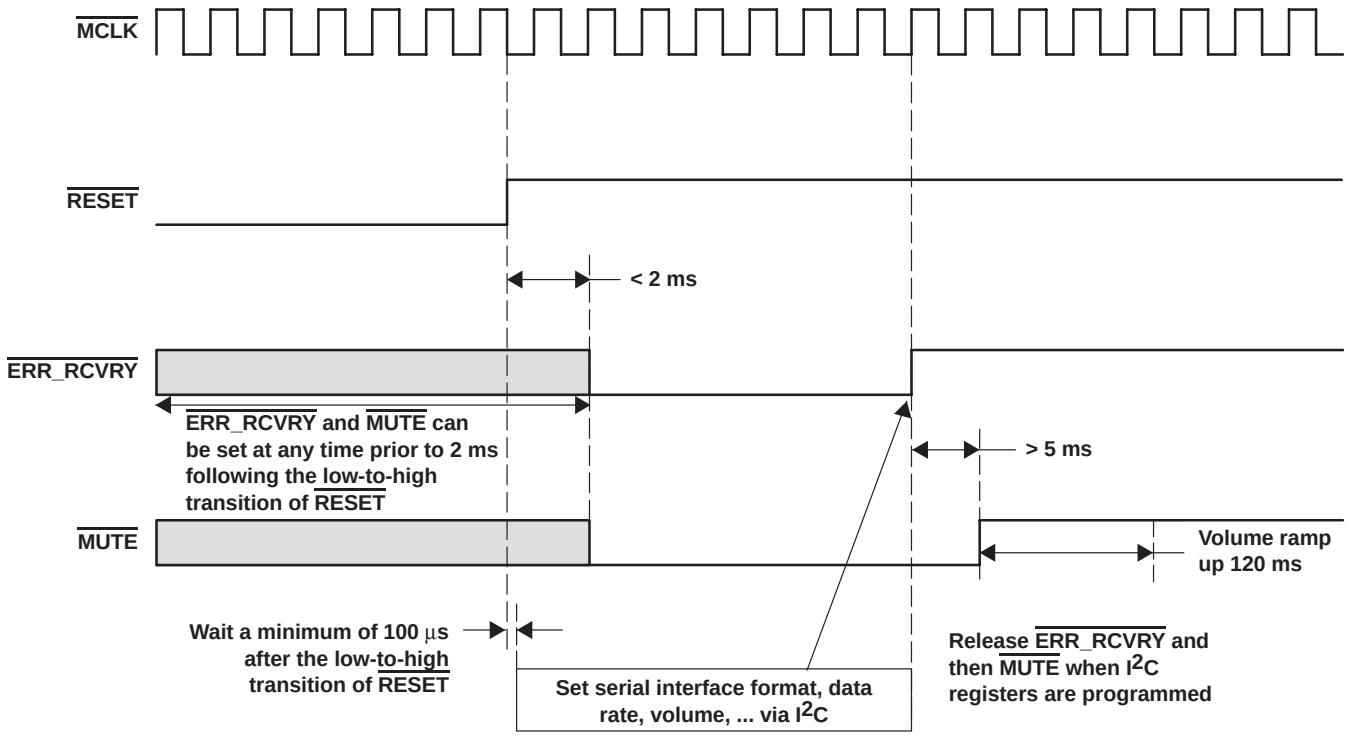



**Figure 4−2. Extending the I²C Write Interval Following Low-to-High Transition of $\overline{\text{RESET}}$ Terminal**

The operation of the TAS5026A can be tailored as desired to meet specific operating requirements by adjusting the following:

- Volume
- Data sample rate
- Emphasis/deemphasis settings
- Individual channel mute
- Automute delay register
- DC-offset control registers

If desired, the TAS5026A can be set to perform an unmute sequence following the low-to-high transition of the $\overline{\text{ERR\_RCVRY}}$ terminal or the error recovery I²C command (register X03 bit D2). This capability is set by writing x7F to the individual error recovery register (x04) and an x84 to x1F (a feature enable register).

## 4.2 Data Sample Rate

If the master clock is well-behaved during the frequency transition (no MCLK_IN high or low clock periods less than 20 ns), then a simple speed selection is performed by setting the DBSPD terminal or the serial control register. If it is known at least 60 ms in advance that the sample rate changes, mute can be used to provide a completely silent transition. The timing of this control sequence is shown in Figure 4−3 and Figure 4−4.

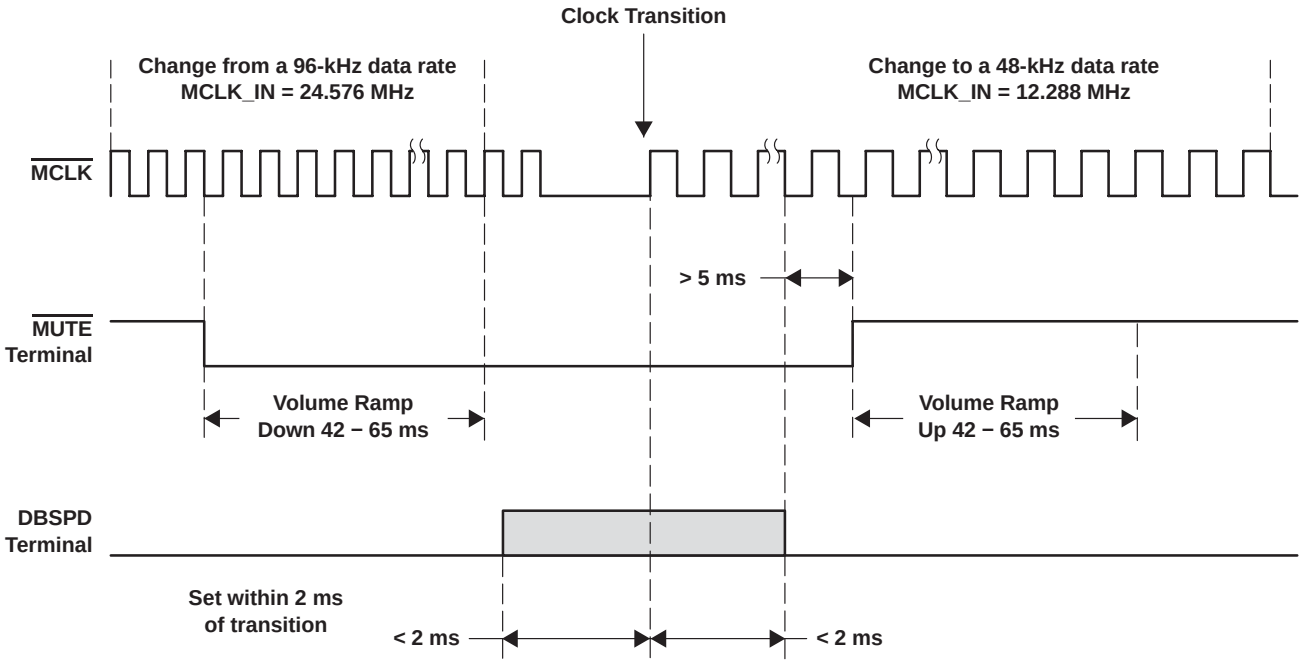



**Figure 4−3. Changing the Data Sample Rate Using the DBSPD Terminal**

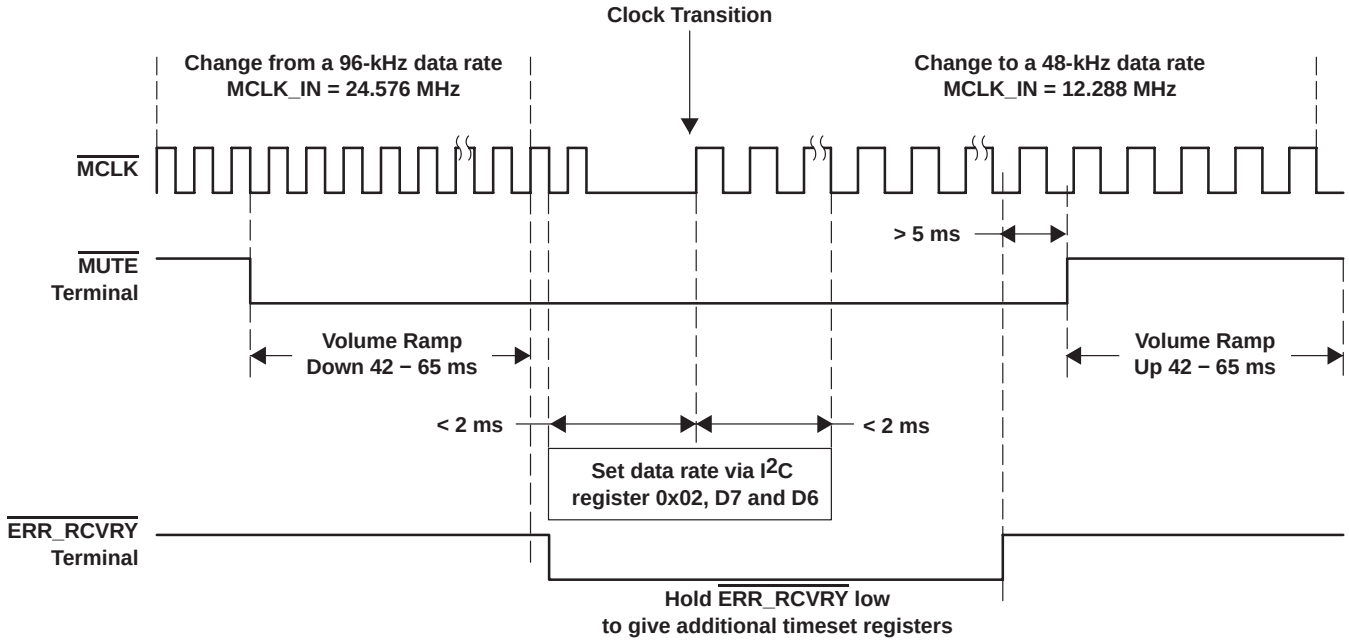



**Figure 4−4. Changing the Data Sample Rate Using the I$^2$C**

However, if the master clock input can encounter a high clock or low clock period of less than 20 ns, then $\overline{\text{RESET}}$ should be applied during this time. There are two recommended control procedures for this case, depending upon whether the DBSPD terminal or the serial control interface is used. These control sequences are shown in Figure 4−5 and Figure 4−6.

Because this sequence employs the $\overline{\text{RESET}}$ terminal, the internal register settings are set to the default values.

Figure 4−5 shows the procedure to change the data rate using the DBSPD terminal and then to restore the register settings. In this example, the $\overline{\text{ERR\_RCVRY}}$ terminal is used to hold off system re-initialization after $\overline{\text{RESET}}$ is released. This permits the system controller to have as much additional time as necessary to restore the register settings.

Once the data rate is set, the $\overline{\text{ERR\_RCVRY}}$ and $\overline{\text{MUTE}}$ terminal signals are set high and the system re-initializes.

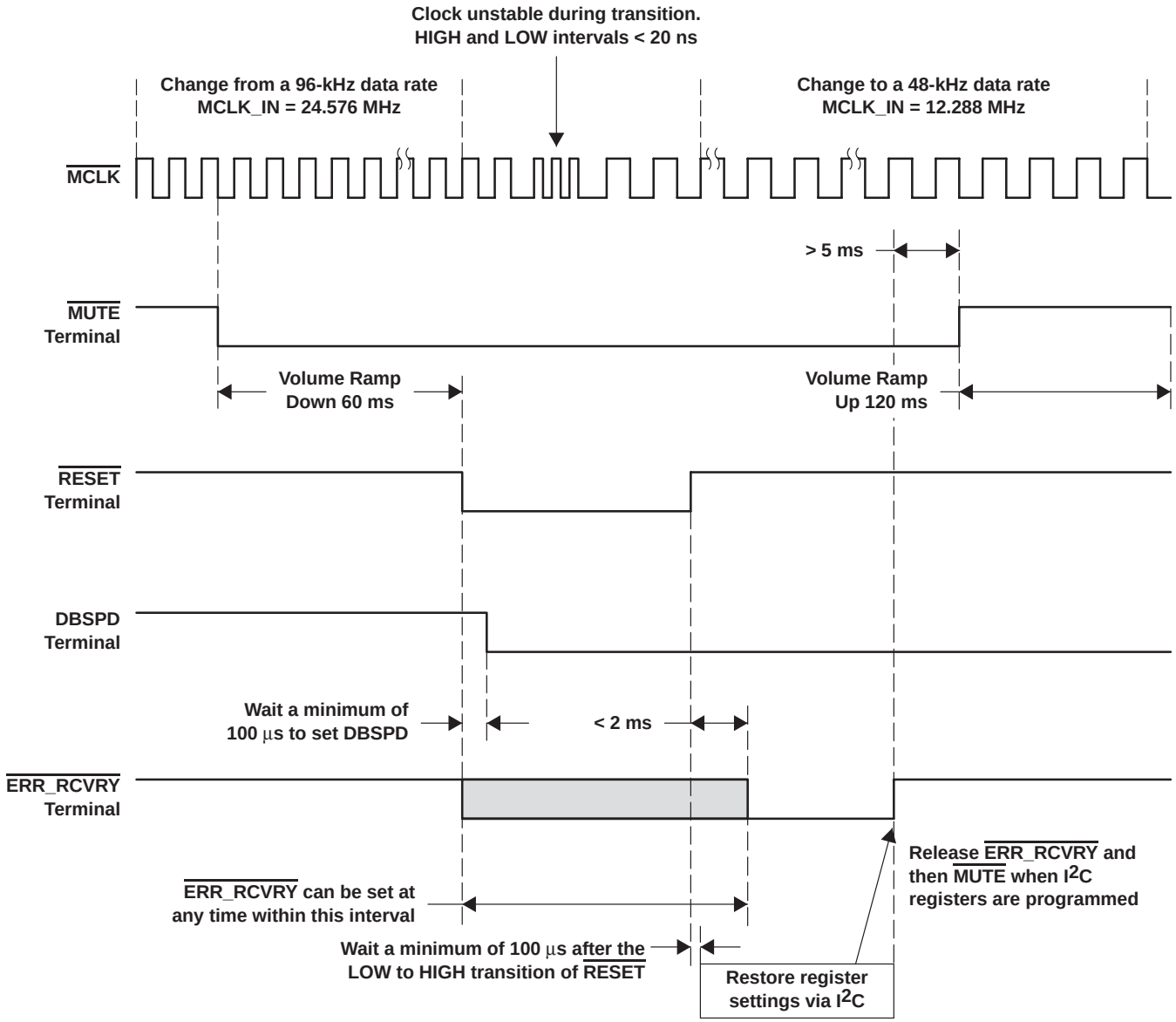



**Figure 4−5. Changing the Data Sample Rate With an Unstable MCLK_IN Using the DBSPD Terminal**

Because this sequence employs the $\overline{\text{RESET}}$ terminal, the internal register settings are set to the default values.

Figure 4−5 shows the procedure to change the data rate using register 0x02 bits D7 and D6 and then to restore the other register settings. In this example, the $\overline{\text{ERR\_RCVRY}}$ terminal is used to hold off system re-initialization after $\overline{\text{RESET}}$ is released. This permits the system controller to have as much additional time as necessary to restore the register settings.

Once the data rate is set, the $\overline{\text{ERR\_RCVRY}}$ and $\overline{\text{MUTE}}$ terminal signals are set high and the system re-initializes.

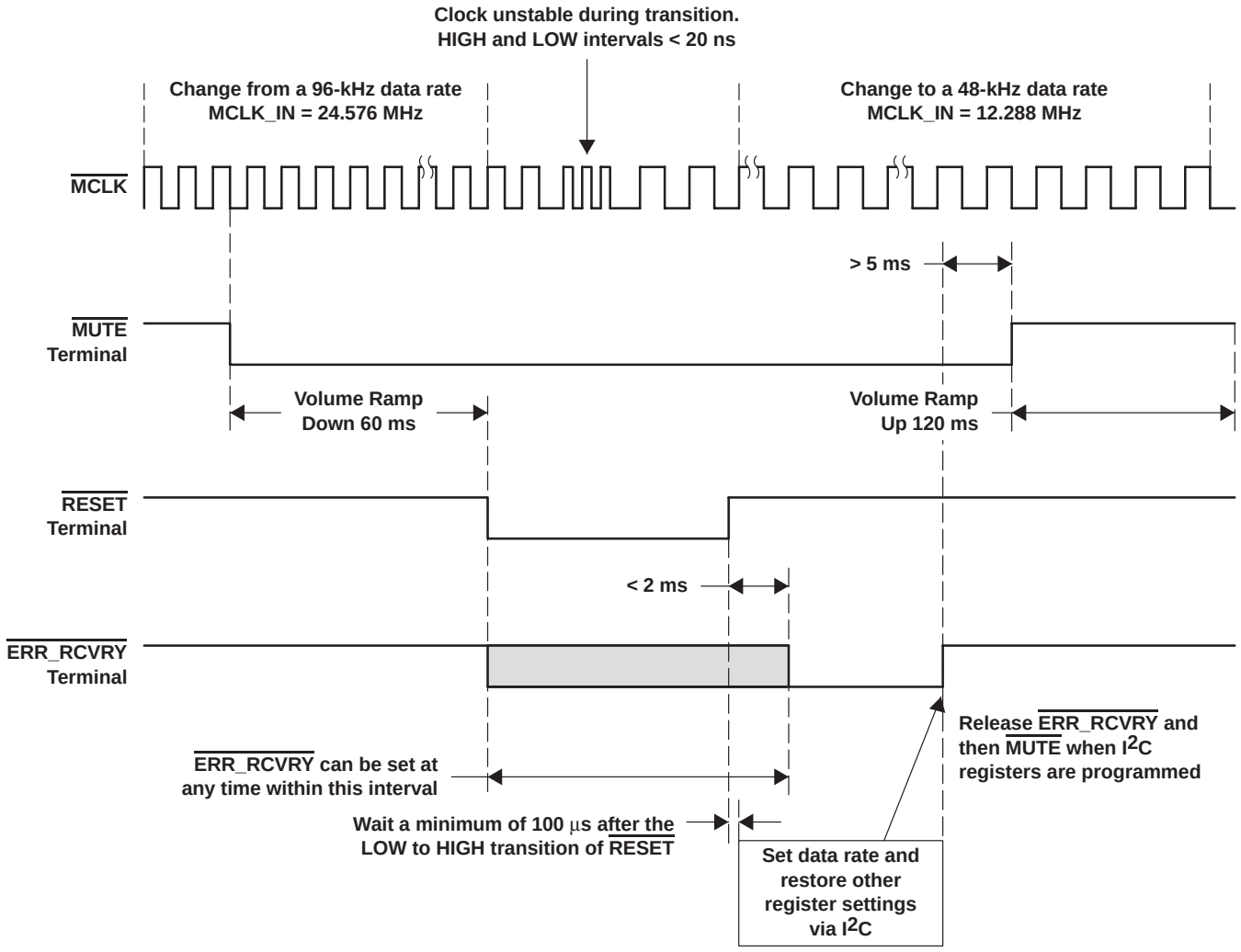



**Figure 4−6. Changing the Data Sample Rate With an Unstable MCLK_IN Using the I²C**

## 4.3 Changing Between Master and Slave Modes

The master and slave mode is set while the $\overline{\text{RESET}}$ terminal is active. Because this sequence employs the $\overline{\text{RESET}}$ terminal the internal register settings are set to the default values.

Figure 4−7 shows the procedure to switch between master and slave modes and then restore the register settings. In this example, the $\overline{\text{ERR\_RCVRY}}$ terminal is used to hold off system re-initialization after $\overline{\text{RESET}}$ is released. This permits the system controller to have as much additional time as necessary to restore the register settings.

Once the data rate is set, the $\overline{\text{ERR\_RCVRY}}$ and $\overline{\text{MUTE}}$ terminal signals are set high and the system re-initializes.

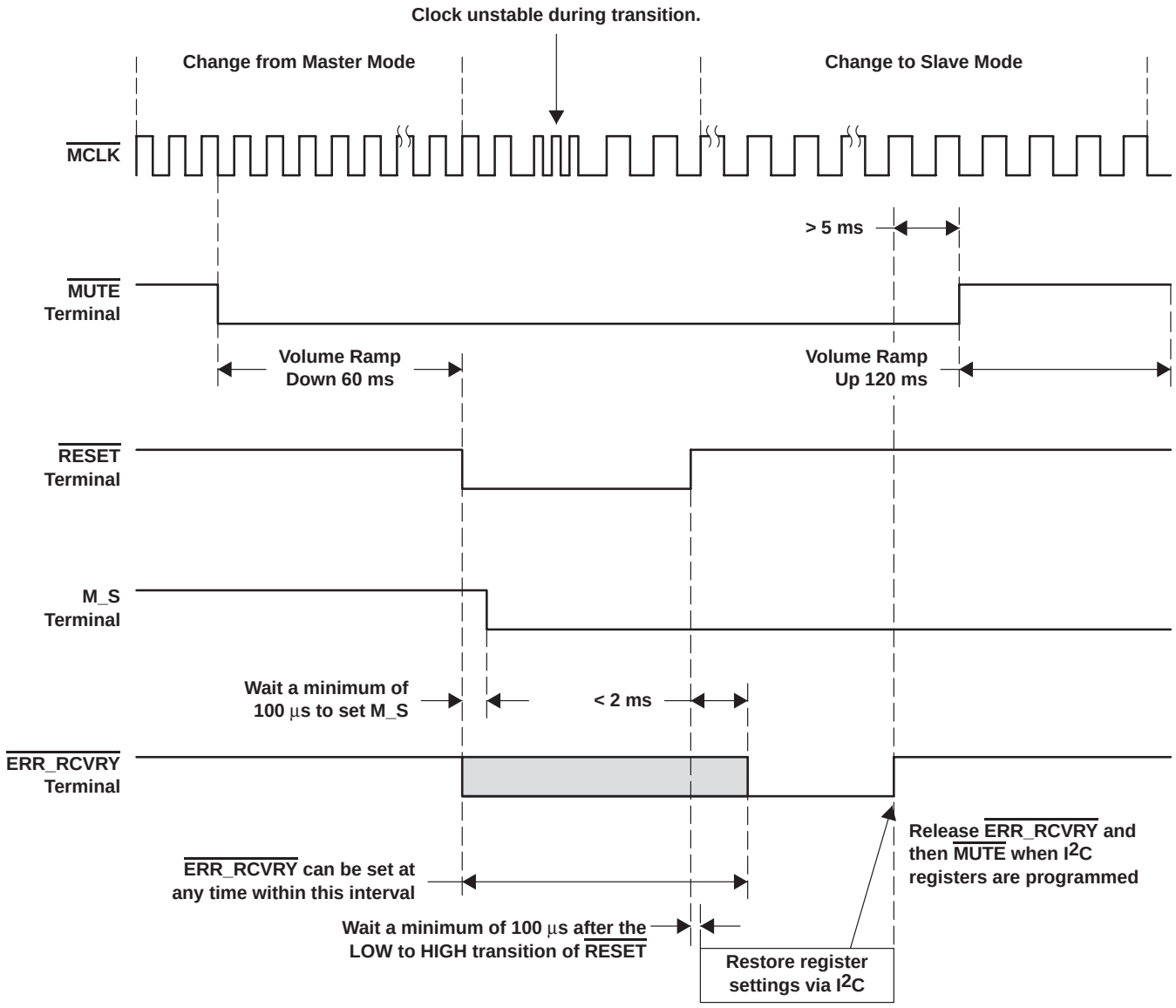



**Figure 4−7. Changing Between Master and Slave Clock Modes**

# 5 Specifications

## 5.1 Absolute Maximum Ratings Over Operating Temperature Ranges (Unless Otherwise Noted)†

Digital supply voltage range: DVDD_CORE, DVDD_PWM, DVDD_RCL . . . . . −0.3 V to 4.2 V
Analog supply voltage range: AVDD_PLL, ADD_OSC . . . . . −0.3 V to 4.2 V
Digital input voltage range, $V_I$ . . . . . −0.3 V to DVDDX + 0.3 V
Operating free-air temperature, TAS5026A . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
ESD . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 Recommended Operating Conditions

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage | Digital | $DV_{DDX}$, See Note 1 | 3 | 3.3 | 3.6 | V |
| Supply current | Digital | Operating | | 60 | | mA |
| | | Power down, See Note 2 | | | 25 | µA |
| Power dissipation | Digital | Operating | | 200 | | mW |
| | | Power down | | | 100 | µW |
| Supply voltage | Analog | $AV_{DDX}$, See Note 3 | 3 | 3.3 | 3.6 | V |
| Supply current | Analog | Operating | | 10 | | mA |
| | | Power down, See Note 2 | | | 25 | µA |
| Power dissipation | Analog | Operating | | 35 | | mW |
| | | Power down, See Note 2 | | | 100 | µW |

NOTES: 3. DVDD_CORE, DVDD_PWM, DVDD_RCL
4. If the clocks are turned off.
5. AVDD_PLL, AVDD_OSC

## 5.3 Electrical Characteristics Over Recommended Operating Conditions

### *5.3.1 Static Digital Specifications Over Recommended Operating Conditions (Unless Otherwise Noted)*

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | DVDD1 | V |
| $V_{IL}$ | Low-level input voltage | | 0 | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_O$ = −1 mA | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_O$ = 4 mA | | 0.4 | V |
| $I_{lkg}$ | Input leakage current | | −10 | 10 | µA |

### *5.3.2 Digital Interpolation Filter and PWM Modulator Over Recommended Operating Conditions (Unless Otherwise Noted) (Fs = 48 kHz)*

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pass band | | 0 | | 20 | kHz |
| Pass band ripple | | | ±0.012 | | dB |
| Stop band | | | 24.1 | | kHz |
| Stop band attenuation | 24.1 kHz to 152.3 kHz | 50 | | | dB |
| Group delay | | | 700 | | µs |
| PWM modulation index (gain) | | | 0.93% | | |

### *5.3.3 TAS5026A/TAS5110 System Performance Measured at the Speaker Terminals Over Recommended Operating Conditions (Unless Otherwise Noted), (Fs = 48 kHz)*

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| SNR (EIAJ) | A-weighted | | 93 | | dB |
| Dynamic range | A-weighted, -60 dB, f = 1 kHz, 20 Hz−20 kHz | | 94 | | dB |
| THD+N | 0 dB, 1 kHz, 20 Hz−20 kHz | | 0.09% | | |

## 5.4 Switching Characteristics

### *5.4.1 Command Sequence Timing*

#### 5.4.1.1 Reset Timing—$\overline{\text{RESET}}$

| CONTROL SIGNAL PARAMETERS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $t_{w(RESET)}$ | Pulses duration, RESET active | | 50 | | | ns |
| $t_{p(VALID\_LOW)}$ | Propagation delay | | | | 1 | µs |
| $t_{p(VALID\_HIGH)}$ | Propagation delay | | 4 | | 5 | ms |
| $t_{d(VOLUME)}$ | Delay time | | 42 | | 65 | ms |

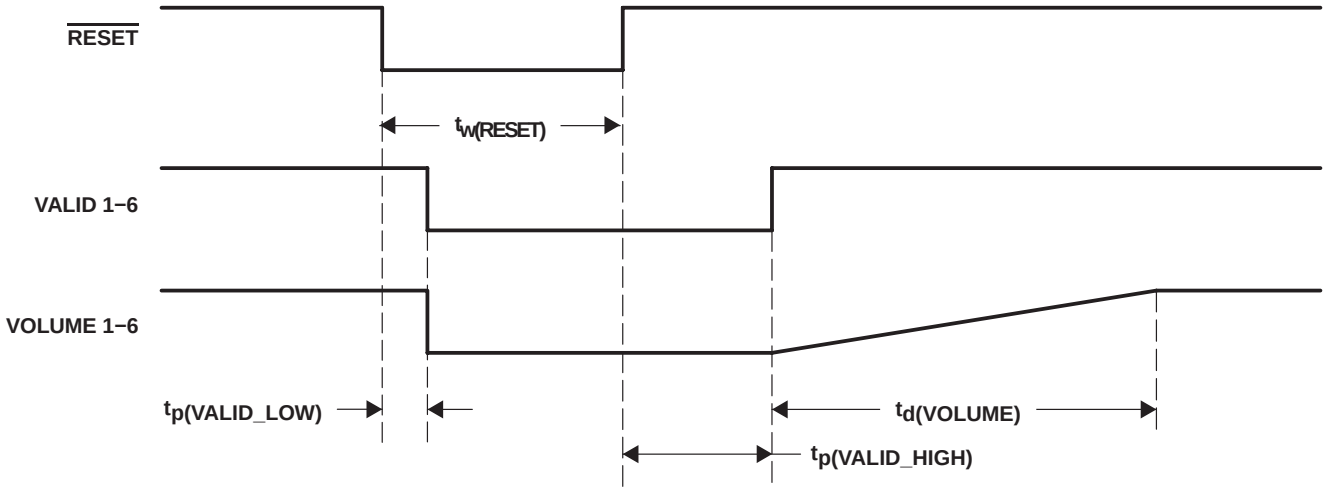



**Figure 5−1. $\overline{\text{RESET}}$ Timing**

### 5.4.1.2 Power-Down Timing—$\overline{\text{PDN}}$

#### *5.4.1.2.1 Long Recovery*

| CONTROL SIGNAL PARAMETERS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $t_{w(PDN)}$ | Pulse duration, $\overline{\text{PDN}}$ active | | 50 | | | ns |
| $t_{d(R\ PDNR)}$ | Reset high to $\overline{\text{PDN}}$ rising edge | | 16 MCLKs | | | ns |
| $t_{p(VALID\_LOW)}$ | | | | | 1 | µs |
| $t_{p(VALID\_HIGH)}$ | | | 85 | | 100 | ms |
| $t_{d(VOLUME)}$ | | | 42 | | 65 | ms |

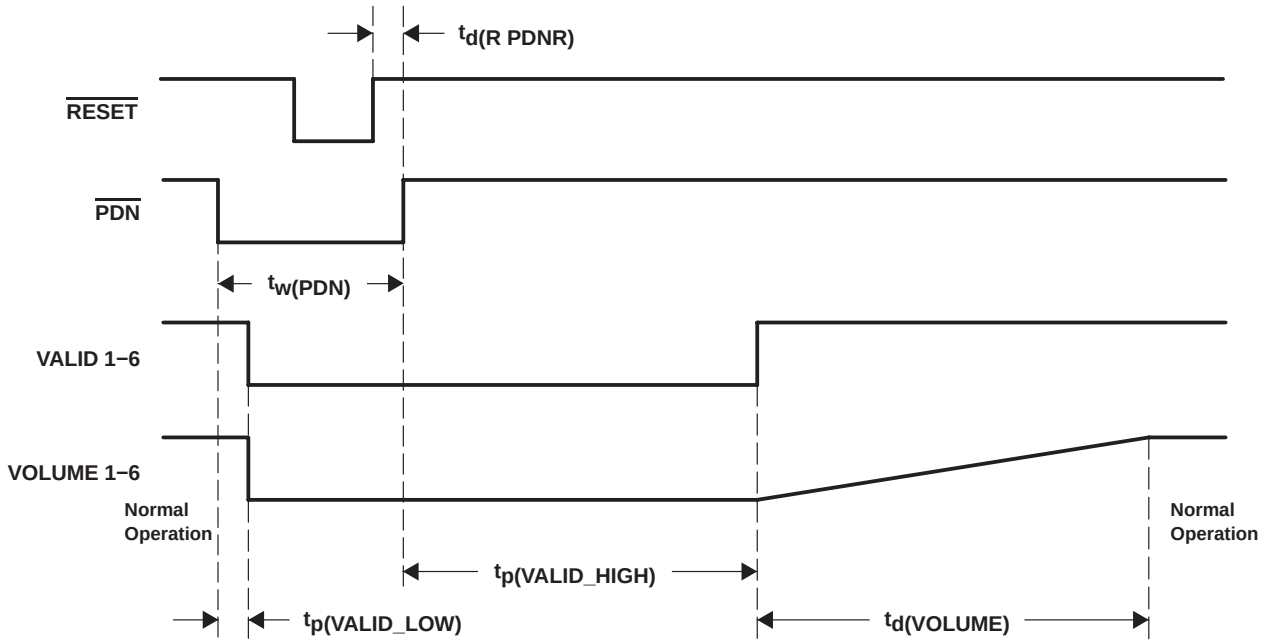



**Figure 5−2. Power-Down and Power-Up Timing—$\overline{\text{RESET}}$ Preceding $\overline{\text{PDN}}$**

#### 5.4.1.2.2 Short Recovery

| CONTROL SIGNAL PARAMETERS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $t_{w(PDN)}$ | Pulse duration, $\overline{PDN}$ active | | 50 | | | ns |
| $t_{d(R\ PDNR)}$ | $\overline{PDN}$ high to reset rising edge | | 16 MCLKs | | | ns |
| $t_{p(VALID\_LOW)}$ | | | | | 1 | µs |
| $t_{p(VALID\_HIGH)}$ | | | 4 | | 5 | ms |
| $t_{d(VOLUME)}$ | | | 42 | | 65 | ms |

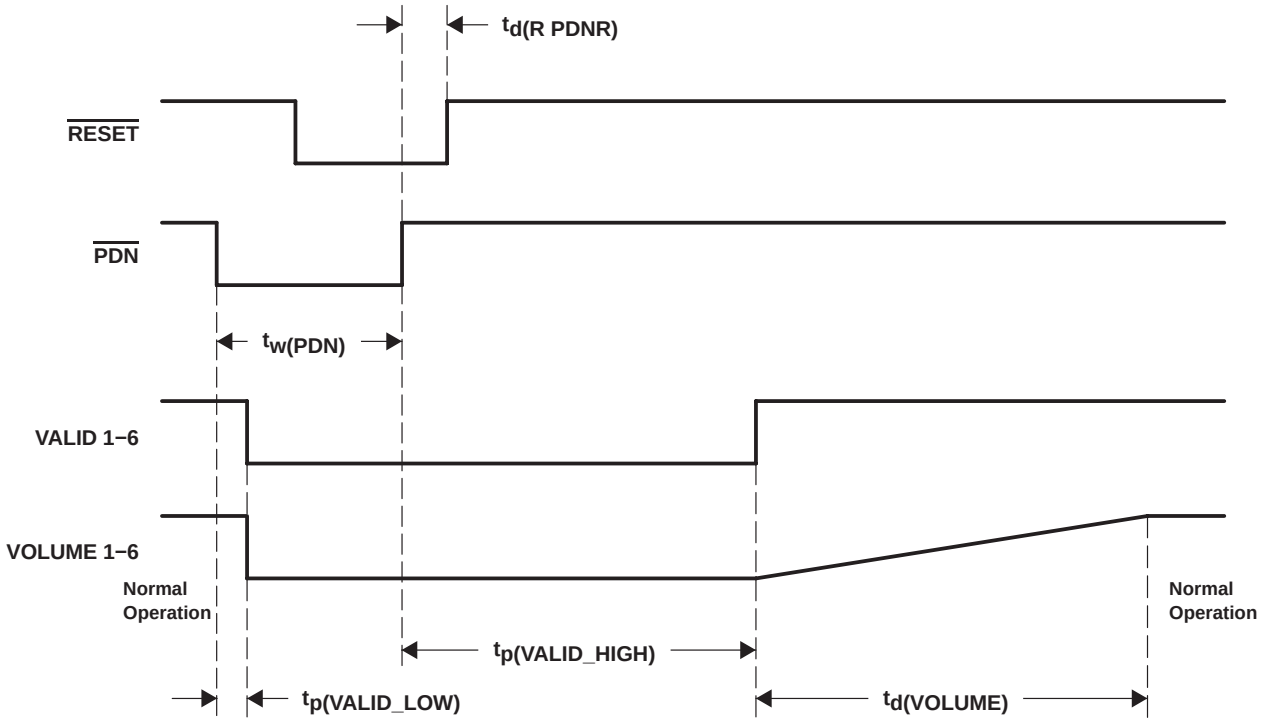



**Figure 5−3. Power-Down and Power-Up Timing—$\overline{RESET}$ Following $\overline{PDN}$**

### 5.4.1.3 Error Recovery Timing—$\overline{ERR\_RCVRY}$

| CONTROL SIGNAL PARAMETERS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $t_{w(ER)}$ | Pulse duration, $\overline{ERR\_RCVRY}$ active | | 5 MCLKs | | | ns |
| $t_{p(VALID\_LOW)}$ | Selectable for minimum or maximum | | 6 | | 47 | µs |
| $t_{p(VALID\_HIGH)}$ | | | 4 | | 5 | ms |

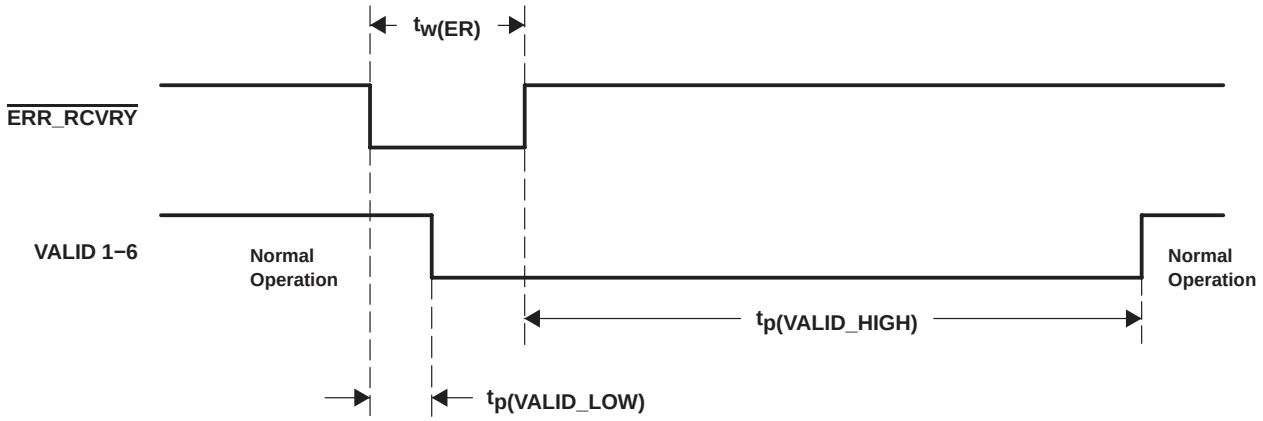



**Figure 5−4. Error Recovery Timing**

### 5.4.1.4 MUTE Timing—$\overline{\text{MUTE}}$

| CONTROL SIGNAL PARAMETERS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $t_{w(MUTE)}$ | Pulse duration, $\overline{\text{PDN}}$ active | | 3 MCLKs | | | ns |
| $t_{d(VOL)}$ | | | | 42 | | ms |

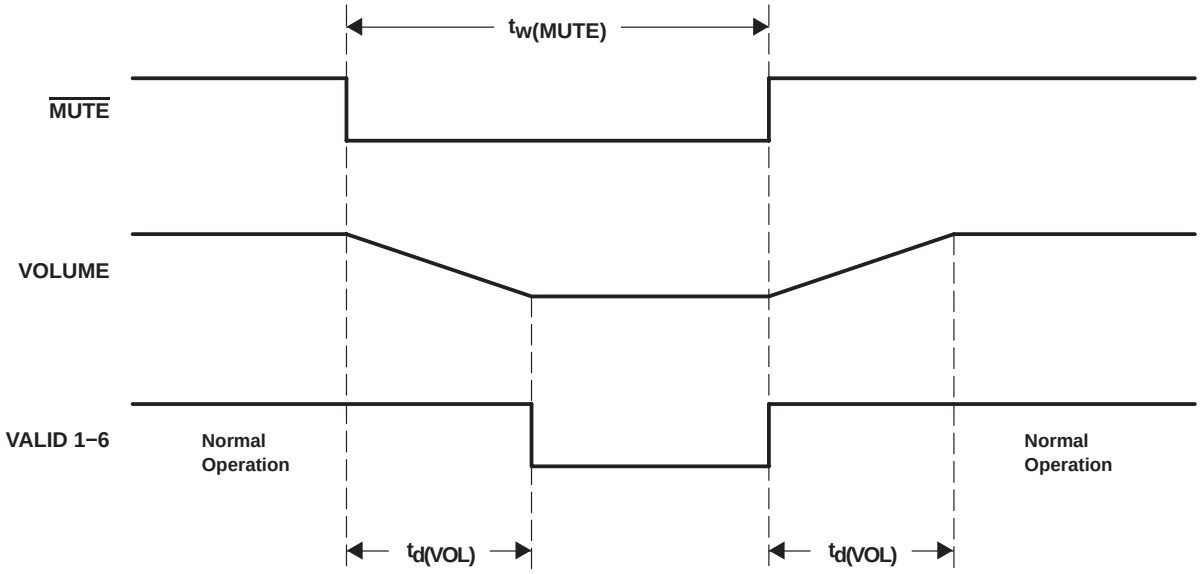



**Figure 5−5. Mute Timing**

## 5.4.2 Serial Audio Port

### 5.4.2.1 Serial Audio Ports Slave Mode Over Recommended Operating Conditions (Unless Otherwise Noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(SCLK)}$ | Frequency, SCLK | | | 12.288 | MHz |
| $t_{su(SDIN)}$ | SDIN setup time before SCLK rising edge | 20 | | | ns |
| $t_{h(SDIN)}$ | SDIN hold time before SCLK rising edge | 10 | | | ns |
| $f_{(LRCLK)}$ | LRCLK frequency | 32 | 48 | 192 | kHz |
| | MCLK_IN duty cycle | | 50% | | |
| | SCLK duty cycle | | 50% | | |
| | LRCLK duty cycle | | 50% | | |
| $t_{su(LRCLK)}$ | LRCLK setup time before SCLK rising edge | 20 | | | ns |
| | MCLK high and low time | 20 | | | ns |

### 5.4.2.2 Serial Audio Ports Master Mode, Load Conditions 50 pF Over Recommended Operating Conditions (Unless Otherwise Noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(MSD)}$ | MCLK_IN to SCLK | 0 | | 5 | ns |
| $t_{(MLRD)}$ | MCLK_IN to LRCLK | 0 | | 5 | ns |

### 5.4.2.3 DSP Serial Interface Mode Over Recommended Operating Conditions (Unless Otherwise Noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(SCLK)}$ | SCLK frequency | | | 12.288 | MHz |
| $t_{d(FS)}$ | Delay time, SCLK rising to Fs | | | | ns |
| $t_{w(FSHIGH)}$ | Pulse duration, sync | | 1/(64×Fs) | | ns |
| $t_{su(SDIN)}$ | SDIN and LRCLK setup time before SCLK falling edge | 20 | | | ns |
| $t_{h(SDIN)}$ | SDIN and LRCLK hold time from SCLK falling edge | 10 | | | ns |
| | SCLK duty cycle | | 50% | | |

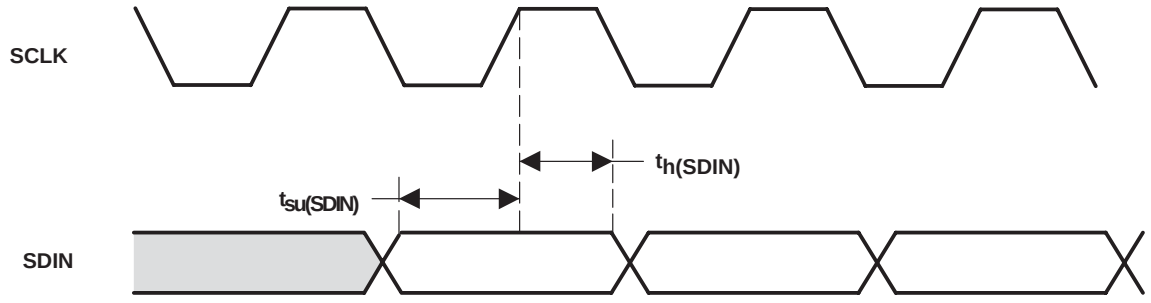
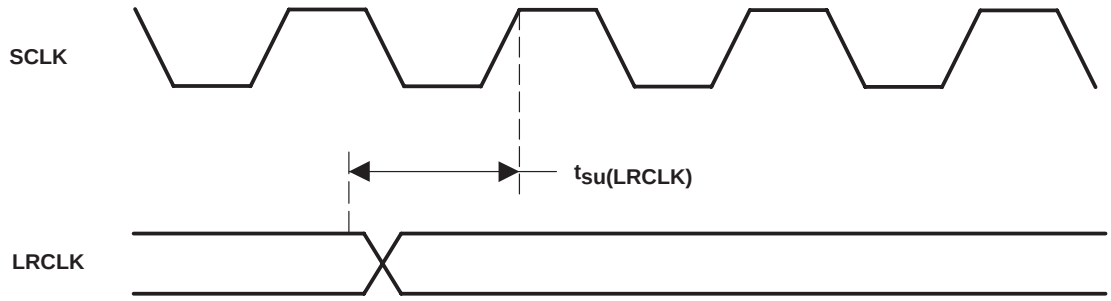



**Figure 5−6. Right-Justified, I²S, Left-Justified Serial-Protocol Timing**




NOTE: Serial data is sampled with the rising edge of SCLK (setup time = 20 ns and hold time = 10 ns).

**Figure 5−7. Right, Left, and I²S Serial-Mode Timing Requirement**

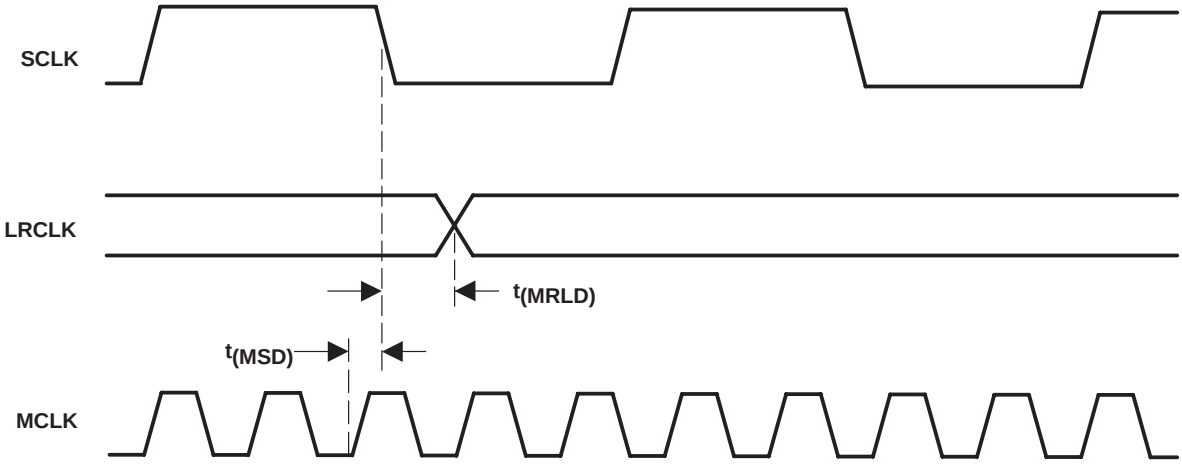



**Figure 5−8. Serial Audio Ports Master-Mode Timing**

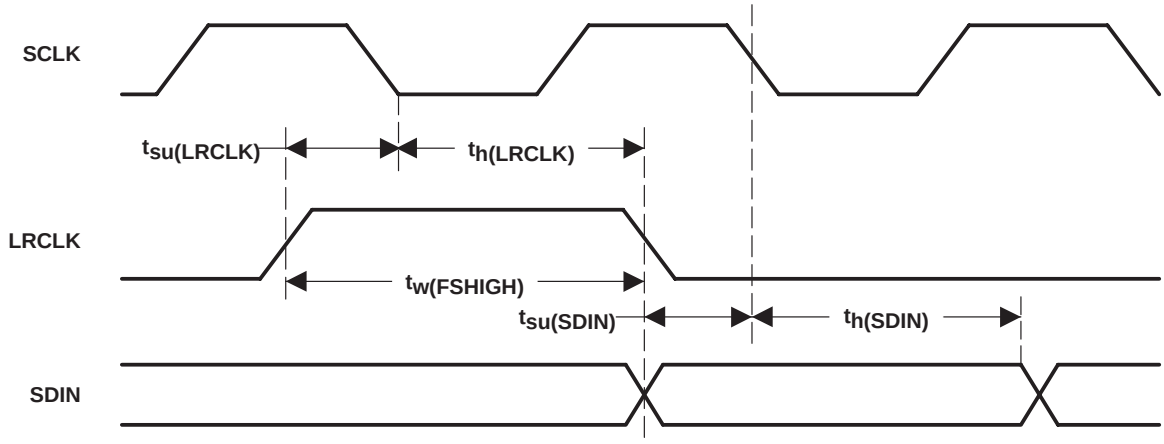



**Figure 5−9. DSP Serial-Port Timing**

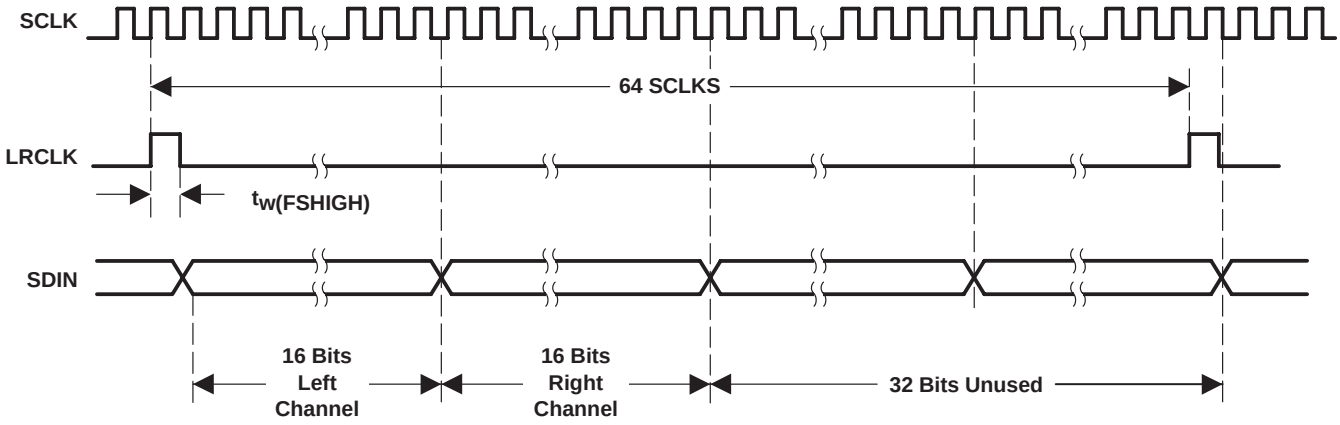



**Figure 5−10. DSP Serial-Port Expanded Timing**

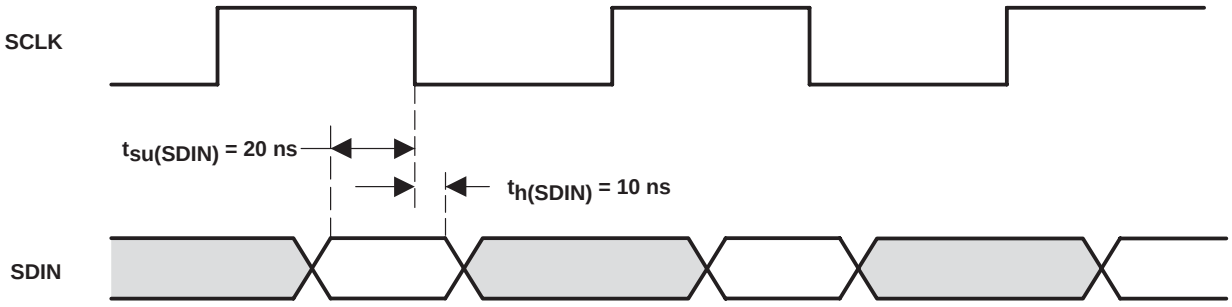



**Figure 5−11. DSP Absolute Timing**

## 5.4.3 Serial Control Port—I²C Operation

### 5.4.3.1 Timing Characteristics for I²C Interface Signals Over Recommended Operating Conditions (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{SCL}$ | Frequency, SCL | | 0 | 100 | 0 | 400 | kHz |
| $t_{w(H)}$ | Pulse duration, SCL high | | 4 | | 0.6 | | µs |
| $t_{w(L)}$ | Pulse duration, SCL low | | 4.7 | | 1.3 | | µs |
| $t_r$ | Rise time, SCL and SDA | | | 1000 | | 300 | ns |
| $t_f$ | Fall time, SCL and SDA | | | 300 | | 300 | ns |
| $t_{su1}$ | Setup time, SDA to SCL | | 250 | | 100 | | ns |
| $t_{h1}$ | Hold time, SCL to SDA | | 0 | | 0 | | ns |
| $t_{(buf)}$ | Bus free time between stop and start condition | | 4.7 | | 1.3 | | µs |
| $t_{su2}$ | Setup time, SCL to start condition | | 4.7 | | 0.6 | | µs |
| $t_{h2}$ | Hold time, start condition to SCL | | 4 | | 0.6 | | µs |
| $t_{su3}$ | Setup time, SCL to stop condition | | 4 | | 0.6 | | µs |
| $C_L$ | Load capacitance for each bus line | | | 400 | | 400 | pF |

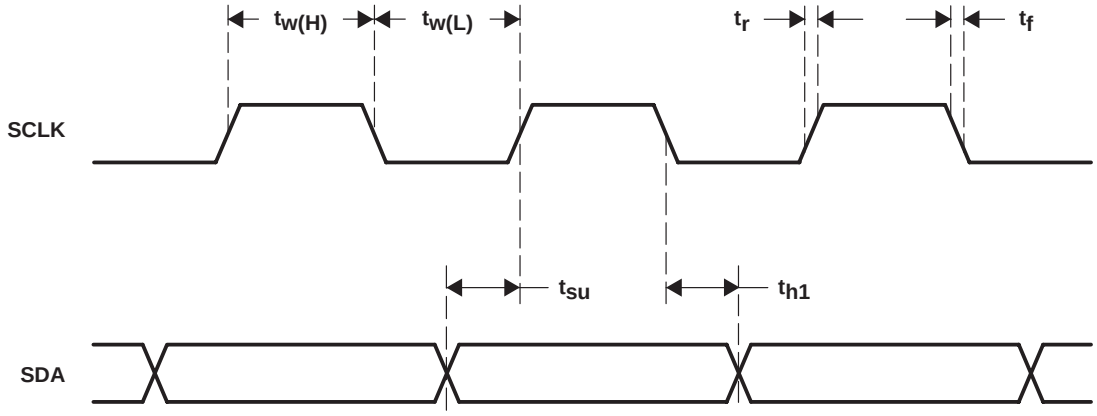



**Figure 5−12. SCL and SDA Timing**

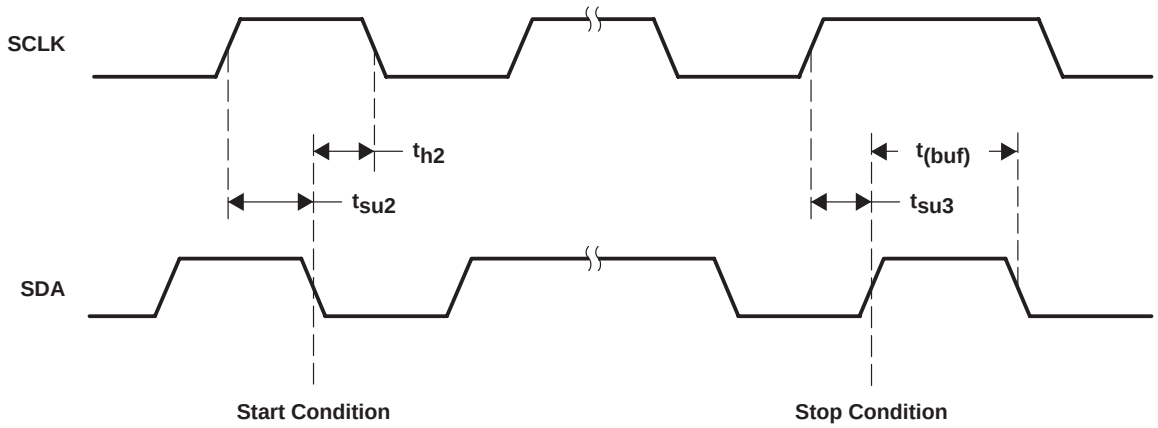



**Figure 5−13. Start and Stop Conditions Timing**

# 6 Application Information

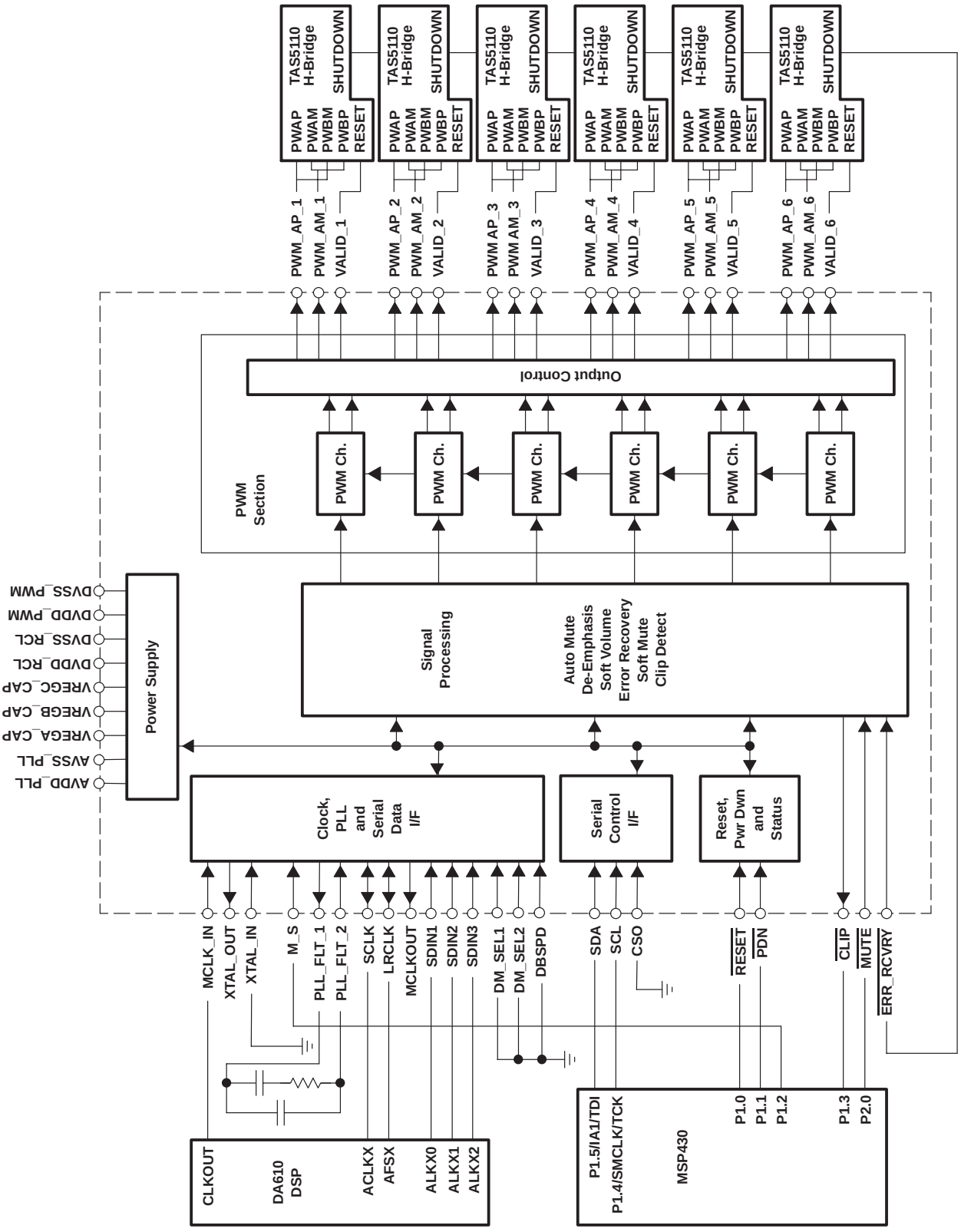



**Figure 6−1. Typical TAS5026A Application**

## 6.1 Serial Audio Interface Clock Master and Slave Interface Configuration

### 6.1.1 Slave Configuration

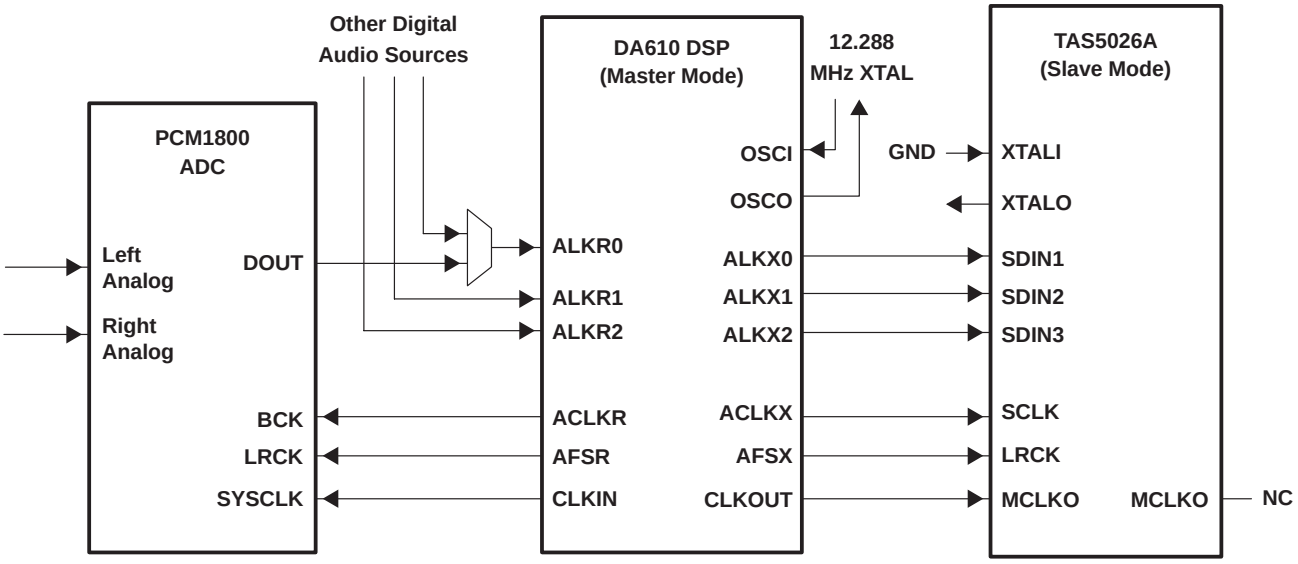



**Figure 6−2. TAS5026A Serial Audio Port—Slave-Mode Connection Diagram**

### 6.1.2 Master Configuration

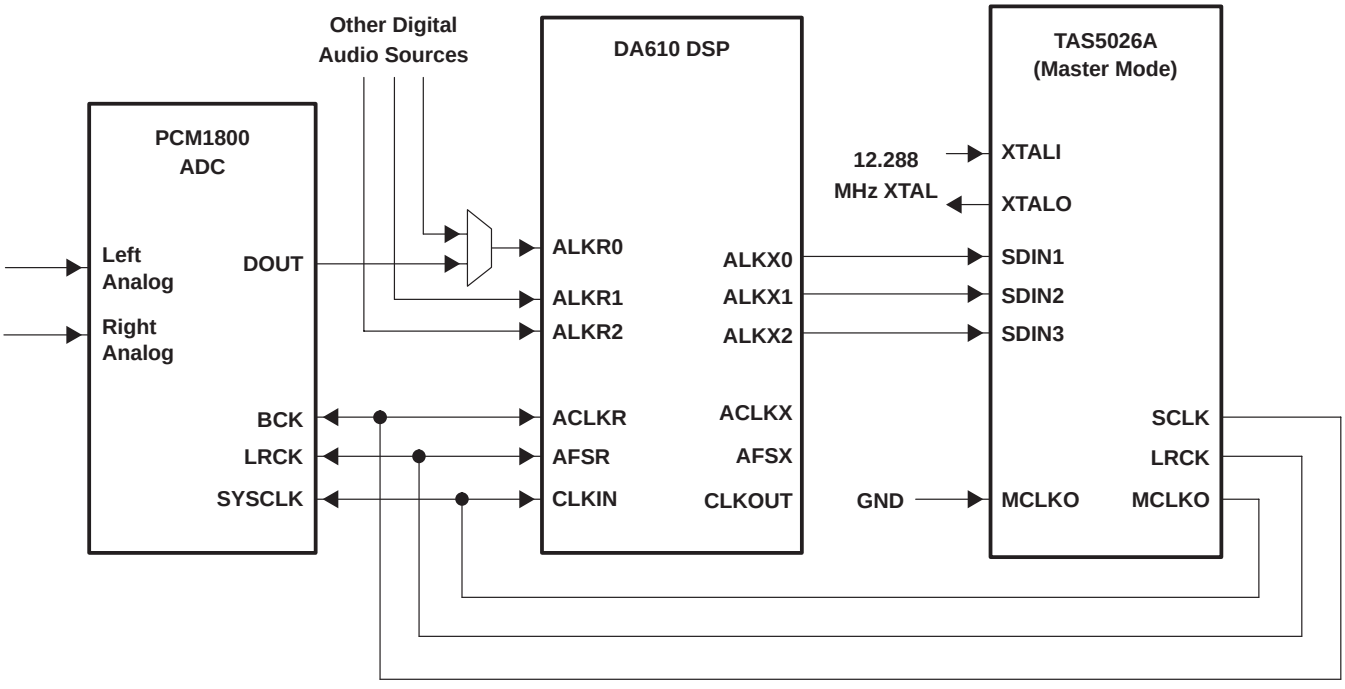
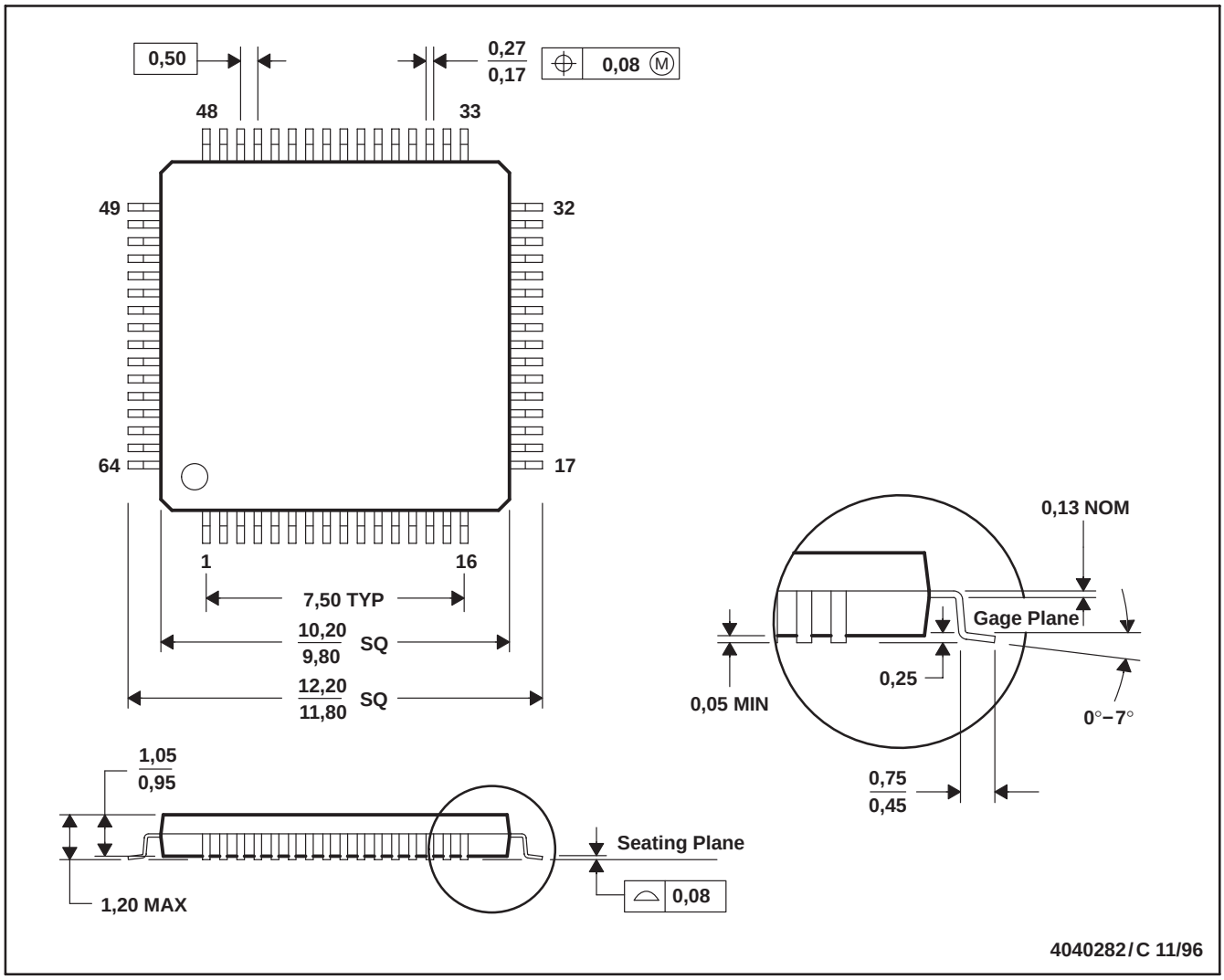



**Figure 6−3. TAS5026A Serial Audio Port—Master-Mode Connection Diagram**

# 7 Mechanical Data

## PAG (S-PQFP-G64) PLASTIC QUAD FLATPACK




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

# Appendix A—Volume Table

| VOLUME SETTING | REGISTER VOLUME (BIN) | GAIN dB |
|---|---|---|
| | D7 − D0 | |
| 249 | 1111 1001 | 24 |
| 248 | 1111 1000 | 23.5 |
| 247 | 1111 0111 | 23 |
| 246 | 1111 0110 | 22.5 |
| 245 | 1111 0101 | 22 |
| 244 | 1111 0100 | 21.5 |
| 243 | 1111 0011 | 21 |
| 242 | 1111 0010 | 20.5 |
| 241 | 1111 0001 | 20 |
| 240 | 1111 0000 | 19.5 |
| 239 | 1110 1111 | 19 |
| 238 | 1110 1110 | 18.5 |
| 237 | 1110 1101 | 18 |
| 236 | 1110 1100 | 17.5 |
| 235 | 1110 1011 | 170 |
| 234 | 1110 1010 | 16.5 |
| 233 | 1110 1001 | 16 |
| 232 | 1110 1000 | 15.5 |
| 231 | 1110 0111 | 15 |
| 230 | 1110 0110 | 14.5 |
| 229 | 1110 0101 | 14 |
| 228 | 1110 0100 | 13.5 |
| 227 | 1110 0011 | 13 |
| 226 | 1110 0010 | 12.5 |
| 225 | 1110 0001 | 12 |
| 224 | 1110 0000 | 11.5 |
| 223 | 1101 1111 | 11 |
| 222 | 1101 1110 | 10.5 |
| 221 | 1101 1101 | 10 |
| 220 | 1101 1100 | 9.5 |
| 219 | 1101 1011 | 9 |
| 218 | 1101 1010 | 8.5 |
| 217 | 1101 1001 | 8 |
| 216 | 1101 1000 | 7.5 |
| 215 | 1101 0111 | 7 |
| 214 | 1101 0110 | 6.5 |
| 213 | 1101 0101 | 6 |
| 212 | 1101 0100 | 5.5 |
| 211 | 1101 0011 | 5 |
| 210 | 1101 0010 | 4.5 |
| 209 | 1101 0001 | 4 |
| 208 | 1101 0000 | 3.5 |
| 207 | 1100 1111 | 3 |
| 206 | 1100 1110 | 2.5 |

| VOLUME SETTING | REGISTER VOLUME (BIN) | GAIN dB |
|---|---|---|
| | D7 − D0 | |
| 205 | 1100 1101 | 2 |
| 204 | 1100 1100 | 1.5 |
| 203 | 1100 1011 | 1 |
| 202 | 1100 1010 | 0.5 |
| 201 | 1100 1001 | 0 |
| 200 | 1100 1000 | −0.5 |
| 199 | 1100 0111 | −1 |
| 198 | 1100 0110 | −1.5 |
| 197 | 1100 0101 | −2 |
| 196 | 1100 0100 | −2.5 |
| 195 | 1100 0011 | −3 |
| 194 | 1100 0010 | −3.5 |
| 193 | 1100 0001 | −4 |
| 192 | 1100 0000 | −4.5 |
| 191 | 1011 1111 | −5 |
| 190 | 1011 1110 | −5.5 |
| 189 | 1011 1101 | −6 |
| 188 | 1011 1100 | −6.5 |
| 187 | 1011 1011 | −7 |
| 186 | 1011 1010 | −7.5 |
| 185 | 1011 1001 | −8 |
| 184 | 1011 1000 | −8.5 |
| 183 | 1011 0111 | −9 |
| 182 | 1011 0110 | −9.5 |
| 181 | 1011 0101 | −10 |
| 180 | 1011 0100 | −10.5 |
| 179 | 1011 0011 | −11 |
| 178 | 1011 0010 | −11.5 |
| 177 | 1011 0001 | −12 |
| 176 | 1011 0000 | −12.5 |
| 175 | 1010 1111 | −13 |
| 174 | 1010 1110 | −13.5 |
| 173 | 1010 1101 | −14 |
| 172 | 1010 1100 | −14.5 |
| 171 | 1010 1011 | −15 |
| 170 | 1010 1010 | −15.5 |
| 169 | 1010 1001 | −16 |
| 168 | 1010 1000 | −16.5 |
| 167 | 1010 0111 | −17 |
| 166 | 1010 0110 | −17.5 |
| 165 | 1010 0101 | −18 |
| 164 | 1010 0100 | −18.5 |
| 163 | 1010 0011 | −19 |
| 162 | 1010 0010 | −19.5 |

| VOLUME SETTING | REGISTER VOLUME (BIN) | GAIN dB |
|---|---|---|
| | D7 – D0 | |
| 161 | 1010 0001 | −20 |
| 160 | 1010 0000 | −20.5 |
| 159 | 1001 1111 | −21 |
| 158 | 1001 1110 | −21.5 |
| 157 | 1001 1101 | −22 |
| 156 | 1001 1100 | −22.5 |
| 155 | 1001 1011 | −23 |
| 154 | 1001 1010 | −23.5 |
| 153 | 1001 1001 | −24 |
| 152 | 1001 1000 | −24.5 |
| 151 | 1001 0111 | −25 |
| 150 | 1001 0110 | −25.5 |
| 149 | 1001 0101 | −26 |
| 148 | 1001 0100 | −26.5 |
| 147 | 1001 0011 | −27 |
| 146 | 1001 0010 | −27.5 |
| 145 | 1001 0001 | −28 |
| 144 | 1001 0000 | −28.5 |
| 143 | 1000 1111 | −29 |
| 142 | 1000 1110 | −29.5 |
| 141 | 1000 1101 | −30 |
| 140 | 1000 1100 | −30.5 |
| 139 | 1000 1011 | −31 |
| 138 | 1000 1010 | −31.5 |
| 137 | 1000 1001 | −32 |
| 136 | 1000 1000 | −32.5 |
| 135 | 1000 0111 | −33 |
| 134 | 1000 0110 | −33.5 |
| 133 | 1000 0101 | −34 |
| 132 | 1000 0100 | −34.5 |
| 131 | 1000 0011 | −35 |
| 130 | 1000 0010 | −35.5 |
| 129 | 1000 0001 | −36 |
| 128 | 1000 0000 | −36.5 |
| 127 | 0111 1111 | −37 |
| 126 | 0111 1110 | −37.5 |
| 125 | 0111 1101 | −38 |
| 124 | 0111 1100 | −38.5 |
| 123 | 0111 1011 | −39 |
| 122 | 0111 1010 | −39.5 |
| 121 | 0111 1001 | −40 |
| 120 | 0111 1000 | −40.5 |
| 119 | 0111 0111 | −41 |
| 118 | 0111 0110 | −41.5 |
| 117 | 0111 0101 | −42 |

| VOLUME SETTING | REGISTER VOLUME (BIN) | GAIN dB |
|---|---|---|
| | D7 – D0 | |
| 116 | 0111 0100 | −42.5 |
| 115 | 0111 0011 | −43 |
| 114 | 0111 0010 | −43.5 |
| 113 | 0111 0001 | −44 |
| 112 | 0111 0000 | −44.5 |
| 111 | 0110 1111 | −45 |
| 110 | 0110 1110 | −45.5 |
| 109 | 0110 1101 | −46 |
| 108 | 0110 1100 | −46.5 |
| 107 | 0110 1011 | −47 |
| 106 | 0110 1010 | −47.5 |
| 105 | 0110 1001 | −48 |
| 104 | 0110 1000 | −48.5 |
| 103 | 0110 0111 | −49 |
| 102 | 0110 0110 | −49.5 |
| 101 | 0110 0101 | −50 |
| 100 | 0110 0100 | −50.5 |
| 99 | 0110 0011 | −51 |
| 98 | 0110 0010 | −51.5 |
| 97 | 0110 0001 | −52 |
| 96 | 0110 0000 | −52.5 |
| 95 | 0101 1111 | −53 |
| 94 | 0101 1110 | −53.5 |
| 93 | 0101 1101 | −54 |
| 92 | 0101 1100 | −54.5 |
| 91 | 0101 1011 | −55 |
| 90 | 0101 1010 | −55.5 |
| 89 | 0101 1001 | −56 |
| 88 | 0101 1000 | −56.5 |
| 87 | 0101 0111 | −57 |
| 86 | 0101 0110 | −57.5 |
| 85 | 0101 0101 | −58 |
| 84 | 0101 0100 | −58.5 |
| 83 | 0101 0011 | −59 |
| 82 | 0101 0010 | −59.5 |
| 81 | 0101 0001 | −60 |
| 80 | 0101 0000 | −60.5 |
| 79 | 0100 1111 | −61 |
| 78 | 0100 1110 | −61.5 |
| 77 | 0100 1101 | −62 |
| 76 | 0100 1100 | −62.5 |
| 75 | 0100 1011 | −63 |
| 74 | 0100 1010 | −63.5 |
| 73 | 0100 1001 | −64 |
| 72 | 0100 1000 | −64.5 |

| VOLUME SETTING | REGISTER VOLUME (BIN) | GAIN dB |
|---|---|---|
| | D7 – D0 | |
| 71 | 0100 0111 | −65 |
| 70 | 0100 0110 | −65.5 |
| 69 | 0100 0101 | −66 |
| 68 | 0100 0100 | −66.5 |
| 67 | 0100 0011 | −67 |
| 66 | 0100 0010 | −67.5 |
| 65 | 0100 0001 | −68 |
| 64 | 0100 0000 | −68.5 |
| 63 | 0011 1111 | −69 |
| 62 | 0011 1110 | −69.5 |
| 61 | 0011 1101 | −70 |
| 60 | 0011 1100 | −70.5 |
| 59 | 0011 1011 | −71 |
| 58 | 0011 1010 | −71.5 |
| 57 | 0011 1001 | −72 |
| 56 | 0011 1000 | −72.5 |
| 55 | 0011 0111 | −73 |
| 54 | 0011 0110 | −73.5 |
| 53 | 0011 0101 | −74 |
| 52 | 0011 0100 | −74.5 |
| 51 | 0011 0011 | −75 |
| 50 | 0011 0010 | −75.5 |
| 49 | 0011 0001 | −76 |
| 48 | 0011 0000 | −76.6 |
| 47 | 0010 1111 | −77 |
| 46 | 0010 1110 | −77.5 |
| 45 | 0010 1101 | −78 |
| 44 | 0010 1100 | −78.5 |
| 43 | 0010 1011 | −79 |
| 42 | 0010 1010 | −79.6 |
| 41 | 0010 1001 | −80.1 |
| 40 | 0010 1000 | −80.6 |
| 39 | 0010 0111 | −81.1 |
| 38 | 0010 0110 | −81.5 |
| 37 | 0010 0101 | −82.1 |

| VOLUME SETTING | REGISTER VOLUME (BIN) | GAIN dB |
|---|---|---|
| | D7 – D0 | |
| 36 | 0010 0100 | −82.6 |
| 35 | 0010 0011 | −83 |
| 34 | 0010 0010 | −83.5 |
| 33 | 0010 0001 | −84 |
| 32 | 0010 0000 | −84.6 |
| 31 | 0001 1111 | −85.1 |
| 30 | 0001 1110 | −85.8 |
| 29 | 0001 1101 | −86.1 |
| 28 | 0001 1100 | −86.8 |
| 27 | 0001 1011 | −87.2 |
| 26 | 0001 1010 | −87.5 |
| 25 | 0001 1001 | −88.4 |
| 24 | 0001 1000 | −88.8 |
| 23 | 0001 0111 | −89.3 |
| 22 | 0001 0110 | −89.8 |
| 21 | 0001 0101 | −90.3 |
| 20 | 0001 0100 | −90.9 |
| 19 | 0001 0011 | −91.5 |
| 18 | 0001 0010 | −92.1 |
| 17 | 0001 0001 | −92.8 |
| 16 | 0001 0000 | −93.6 |
| 15 | 0000 1111 | −94.4 |
| 14 | 0000 1110 | −95.3 |
| 13 | 0000 1101 | −96.3 |
| 12 | 0000 1100 | −97.5 |
| 11 | 0000 1011 | −98.8 |
| 10 | 0000 1010 | −100.4 |
| 9 | 0000 1001 | −102.4 |
| 8 | 0000 1000 | −104.9 |
| 7 | 0000 0111 | −108.4 |
| 6 | 0000 0110 | −114.4 |
| 5 | 0000 0101 | MUTE |
| 4 | 0000 0100 | MUTE |
| 3 | 0000 0011 | MUTE |
| 2 | 0000 0010 | MUTE |
| 1 | 0000 0001 | MUTE |
| 0 | 0000 0000 | MUTE |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TAS5026APAG | NRND | TQFP | PAG | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR |
| TAS5026APAGG4 | NRND | TQFP | PAG | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR |
| TAS5026APAGR | NRND | TQFP | PAG | 64 | 1500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR |
| TAS5026APAGRG4 | NRND | TQFP | PAG | 64 | 1500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR |

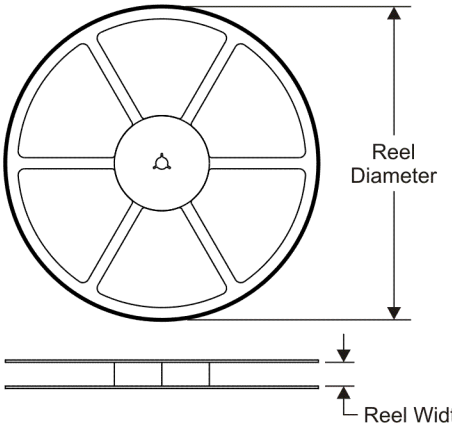
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

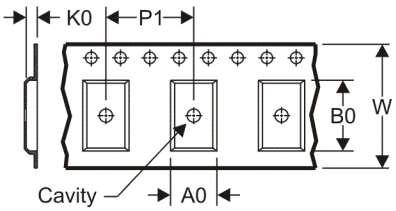
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

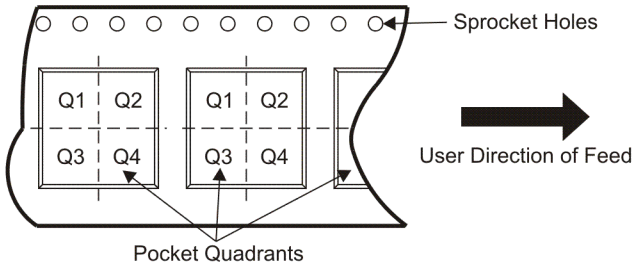



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

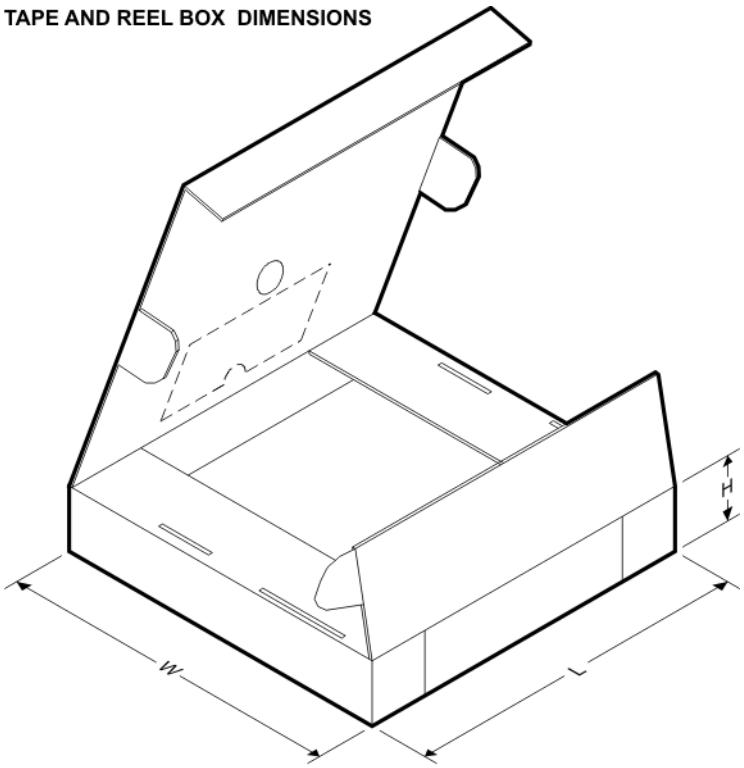
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5026APAGR | TQFP | PAG | 64 | 1500 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |

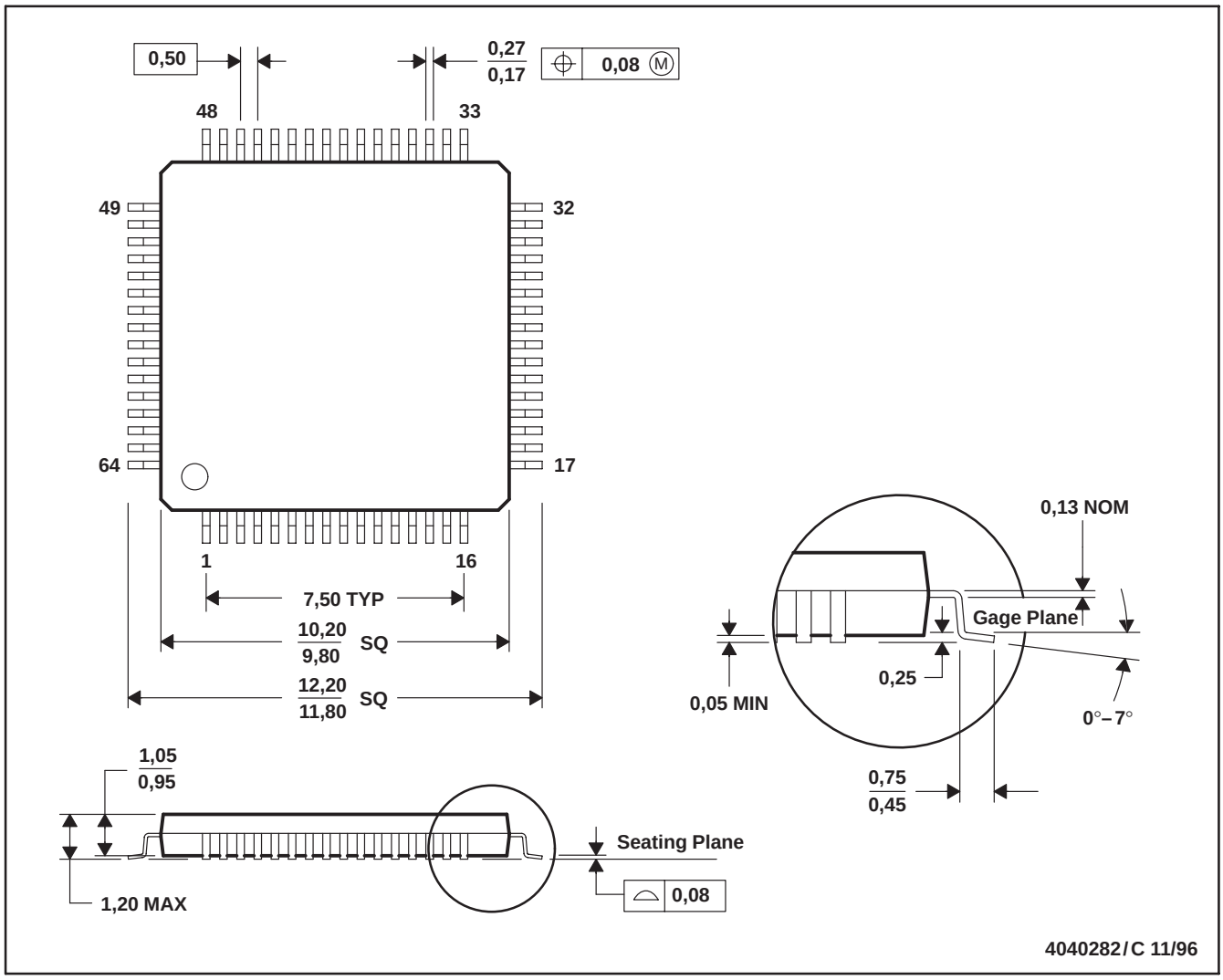
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TAS5026APAGR | TQFP | PAG | 64 | 1500 | 346.0 | 346.0 | 41.0 |

**PAG (S-PQFP-G64)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026